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THESIS

MIXED SIGNAL PROCESSOR FOR A ROBUST
SYMMETRICAL NUMBER SYSTEM DIRECTION FINDING
ANTENNA

by

Charles F. Babb

September 2002

Thesis Advisor:
Co-Advisor:

Phillip E. Pace
David C. Jenn

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**MIXED SIGNAL PROCESSOR FOR A ROBUST SYMMETRICAL NUMBER
SYSTEM DIRECTION FINDING ANTENNA**

Charles F. Babb
Lieutenant, United States Navy
B.S., Auburn University, 1995

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Author: Charles F. Babb

Approved by: Phillip E. Pace
Thesis Advisor

David C. Jenn
Co-Advisor

Dan C. Boger
Chairman, Department of Information Sciences

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ABSTRACT

This applied research project has designed, simulated, constructed and tested the performance of a processing system for a prototype direction finding antenna. A mixed signal architecture to derive the direction of arrival from a Robust Symmetrical Number System (RSNS) encoded direction finding array is based on a new phase sampling interferometer approach that can be easily incorporated into established techniques to provide a high resolution, small-baseline array with few number of phase sampling comparators. The approach is based on preprocessing the received signal using the RSNS. The preprocessing is used to decompose the spatial filtering operation into a number of parallel suboperations (moduli) that are of smaller computational complexity. A much higher direction finding spatial resolution is achieved after the N different moduli are used and the results of the low precision suboperations are recombined, in addition to the reduction of the number of possible encoding errors due to the RSNS' inherent Gray-coding properties. This has resulted in a four inch antenna array being able to attain an angular resolution of less than 1.8 degrees with a continuous field of view of 120 degrees. The accompanying electronics occupy two 6 inch by 8 inch printed circuit boards, making this system ideal for platforms with limited space and volume.

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I. INTRODUCTION

A. DIRECTION FINDING SYSTEMS

Direction Finding (DF) systems find applications in many areas. Wildlife management, telecommunications personnel, law enforcement and the military all have important applications that require knowledge of the direction of radio signals. Radio DF systems generally take advantage of a known antenna response to incident plane waves in order to estimate the angle of arrival (AOA) of a signal. Performance measures of a DF system include accuracy, resolution, bandwidth, signal-to-noise ratio, field of view (FOV), and physical attributes (size, weight, geometrical shape, etc.). Another consideration is the processing electronics or computational resources necessary to extract the angle information from the antenna signal [1]. This thesis describes a DF system that provides a high-resolution, small baseline array with fewer number of phase sampling comparators (i.e., reduced electronics) and a circuit board with a relatively small footprint.

The approach presented in this thesis is based on preprocessing the received signal using Symmetrical Number System (SNS) encoding of the antenna waveform. The Optimum Symmetrical Number System (OSNS) approach is presented in the work of Hatziathanasiou [2]. Improvements on the OSNS resulted in the Robust Symmetrical Number System (RSNS) approach was addressed in the work of Wickersham [3] and York [4], and is extended here. The SNS preprocessing is used to decompose the spatial filtering operation into a number of parallel sub-operations, N , that are of smaller computational complexity. Each sub-operation is a

separately configured interferometer whose phase output is a symmetrically folded waveform that folds at an integer multiple of the modulus. A small comparator ladder mid-level quantizes each folded phase response. Consequently, each sub-operation only requires a precision in accordance with that modulus. A much higher DF spatial resolution is achieved after the results of these low precision sub-operations are recombined. By incorporating the OSNS or RSNS preprocessing concept, the field of view (FOV) of a specific configuration of interferometers and phase sampling comparator arrangements can be analyzed exactly, without ambiguity [1].

B. PRINCIPAL CONTRIBUTIONS

This thesis has focused on the design and manufacture of an improved RSNS Signal Processing Circuit to operate in conjunction with a previously constructed antenna. Principal contributions consist of improved and simplified digital processing with a reduction in the accompanying analog circuitry's size. A digital readout in degrees was also added to enable instant visual readability.

The previous RSNS Signal Processing Circuit was designed and implemented utilizing Electrically Erasable Programmable Read-Only Memory (EEPROM) chips, necessitating a large amount of electronic overhead and complex digital processing. The previous approach also precluded a comprehensive computer simulation of the circuit in its entirety because the available design software contained program limitations that did not allow simulation of the circuit as a unit. Results from the previous design had significant errors in the final transfer function, but

proved the viability of the system and provided sufficient impetus to continue the project. The current design utilizes combinational logic in its simplest forms, thus reducing complexity and probability for error in digital processing. Simulation was completed for the current digital processor in its entirety with excellent results.

The analog portion of the new RSNS Signal Processing Circuit was designed with high accuracy and compact electronics as priorities. To this end, integrated circuit chips were selected that contained more than one electronic component and have internally implemented functions such as hysteresis and pull-up resistors. This resulted in the RSNS Signal Processing Circuit occupying two printed circuit boards (PCBs) measuring 6 inches by 8 inches each.

A digital readout was added at the processor output to allow instant visual readability by an operator. This display includes an error indication feature that actuates when the digital logic determines that the analog signals do not correspond to an AOA within the system's FOV.

C. THESIS OUTLINE

Chapter II of this thesis provides a brief review of phase sampled interferometry. Chapter III describes the RSNS and the work of York [4] and Wickersham [3]. This chapter presents previous work done in DF antenna systems. Chapter IV presents the current design and implementation for an improved RSNS Signal Processing Circuit. Chapter V details the testing and evaluation performed to validate the RSNS Signal Processing Circuit both before and after manufacture. Chapter VI presents conclusions of this project and proposes some avenues for future work.

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II. PHASE SAMPLED INTERFEROMETRY

A two-element linear array is shown in Figure 2.1. The two antenna elements are spaced a distance d apart and the incident plane wave arrives with bearing angle θ_B , which can take on values $\pi/2 > \theta_B > -\pi/2$ in the visible region. The antenna response to an incident plane wave can be cast in the form of a sinusoidal function of θ_B , which is a folding waveform.

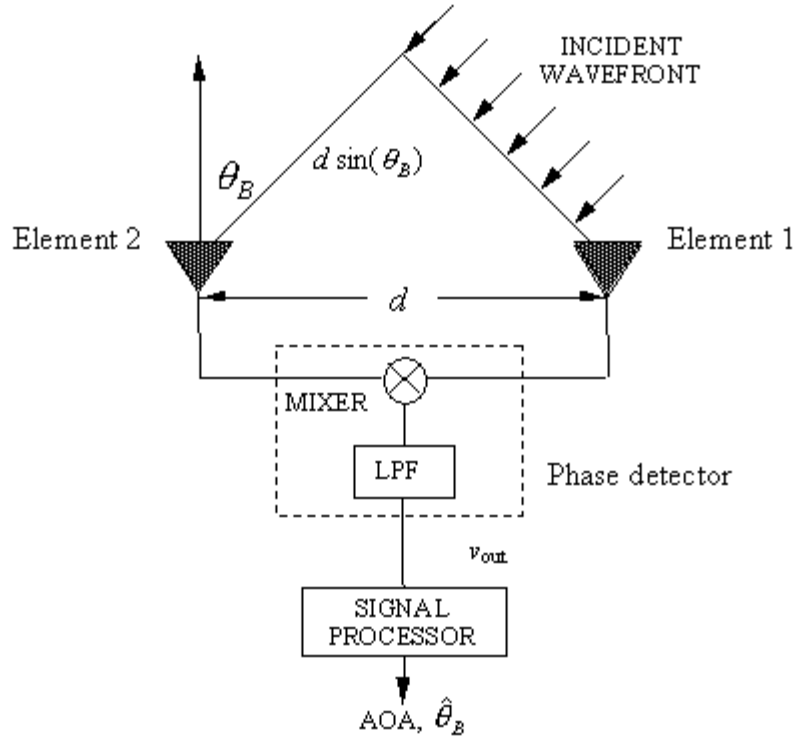


Figure 2.1: Two-Element Interferometry. [From Ref 1]

There are several ways of generating a folding waveform at the array output. Although conventional beamforming (i.e., summing the element outputs) provides a sinusoidal output vs. incidence angle, the amplitude of the

antenna output is not constant due to the element factor. Variable gain amplifiers could be added at each element to provide constant output. Digital beamforming using a coherent detector at each element would also provide a means of generating a folding waveform. One method of obtaining a constant amplitude folding waveform is detailed in Figure 2.1. The individual element outputs are amplified then mixed (multiplied together and lowpass filtered), resulting in an output signal whose frequency is the difference of the two input signal frequencies. Because the signals have the same frequency, the mixer output voltage is

$$v_{out} = \frac{V^2}{2} \cos(kd \sin(\theta_B)) \quad (2.1)$$

where $k = \frac{2\pi}{\lambda}$, V is the maximum value of the voltage at the antenna elements, and λ is the wavelength.

The output voltage is a periodic waveform that contains the plane wave AOA information. Ambiguities are generated for baselines where $d > \lambda/2$. That is, the output voltage is highly ambiguous with a single value of voltage corresponding to many angles of arrival. The number of folding periods n that occur within an AOA of π radians is $n = \frac{2d}{\lambda}$. For example, with $d = 7.5\lambda$, $n = 15$ folds are available in the visible region.

The ambiguities within the symmetrical folding waveform can be resolved by using additional interferometers in the linear array. A common approach is to have each interferometer in the linear array symmetrically fold the antenna response with the folding period between interferometers being a successive factor of

two, for example $d_4 = 2d_3 = 4d_2 = 8d_1$. High-speed binary comparators can then be used to produce a digital Gray code output. The folding waveforms are shifted appropriately using a phase shifter in each channel to achieve the Gray code result. The folded output from each phase detector is then quantized with a single comparator with a normalized threshold level $T = 0.5$. Together, the comparator outputs directly encode the signal's AOA in the Gray code format. This approach makes use of the periodic dependence of the interferometer's phase response on the incident plane wave's AOA and the distance between the elements of each interferometer.

One of the major limitations associated with the above approach is the achievable resolution for a fixed maximum baseline. For the folding periods to be a successive factor of 2, the distance between the elements must also be doubled. That is, an 8-bit DF antenna using the previous scheme would require element spacings $\lambda/4, \lambda/2, \lambda, \dots, 32\lambda$ with a total baseline length of 32λ . This distance-doubling of the element spacings requires complex analog hardware and adversely affects the physical implementation of the DF architecture. This doubling also gains only one digital bit of information per interferometer and ultimately constrains the achievable resolution [5].

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III. PREVIOUS RSNS DIRECTION FINDING SYSTEMS

A. ROBUST SYMMETRICAL NUMBER SYSTEM BACKGROUND

In the RSNS, N different periodic symmetrical waveforms are used with pairwise relatively prime integers m_1, m_2, \dots, m_N . The RSNS is based on the following sequence

$$\bar{x}_{m_l} = [0, 1, 2, \dots, m-1, m, m-1, \dots, 2, 1] \quad (3.1)$$

where \bar{x}_{m_l} is a row vector and m is a positive integer ($m > 0$) [6]. In an N -channel RSNS, where $N \geq 2$, the basic sequence for the i^{th} channel (modulus m) is

$$\bar{x}_{m_2} = [0, 0, \dots, 0, 0, 1, 1, \dots, 1, 1, \dots, m, m, \dots, m, m, \dots, 1, 1, \dots, 1, 1] \quad (3.2)$$

In this sequence each value in the \bar{x}_{m_l} row vector is put N times in succession. This sequence is repeated in both directions, forming a periodic sequence with the period

$$P_{RSNS} = 2mN \quad (3.3)$$

Considering a single channel, the discrete states of the robust symmetrical number system can be expressed as [6]

$$g = \begin{cases} \left\lfloor \frac{n-s_i}{N} \right\rfloor, & s_i \leq n \leq Nm_i + s_i + 1 \\ \left\lfloor \frac{2Nm_i + N - n + s_i - 1}{N} \right\rfloor, & Nm_i + s_i + 2 \leq n \leq 2Nm_i + s_i - 1 \end{cases} \quad (3.4)$$

where g is the n^{th} term of channel i , m_i is the channel modulus, s_i is a corresponding sequence shift $s_i \equiv 0, 1, 2, \dots, N-1 \pmod{N}$ and $N \geq 2$ is the number of channels in the system. The values $\{s_1, s_2, \dots, s_N\}$ must form a complete residue system modulo N . Because of the relative property of the

shifts, one of the shift values will be set equal to 0. The index n corresponds to the input value. The discrete states of the RSNS are indexed using the $s_i=0$ row vector with the index starting from the first zero. Note that the largest integer within each periodic sequence is the modulus m .

An N -channel RSNS is formed of vectors by picking N moduli m_i , and N shift values s_i , $1 \leq i \leq N$. Since the fundamental period for channel i is $2Nm_i$, it follows that the period for the RSNS vectors must be a multiple of $2Nm_i$. Therefore the fundamental period for the RSNS is [6]

$$PF_{RSNS} = [2m_1N, 2m_2N, \dots, 2m_NN] \quad (3.5)$$

where $[a_1, a_2, \dots, a_N]$ is the least common multiple of a_1, a_2, \dots, a_N . From number theory

$$PF_{RSNS} = 2N[m_1, m_2, \dots, m_N] \quad (3.6)$$

To illustrate the RSNS, Figure 3.1 shows the folding waveform and integer values within each modulus for $m_1=5$ (shift $s_1=0$) $m_2=6$ (shift $s_2=1$). Note the Gray-code properties from one code transition to the next. The thresholds shown on the vertical axis represent the integer values within each RSNS modulus. The integer values occur $N=2$ times in succession.

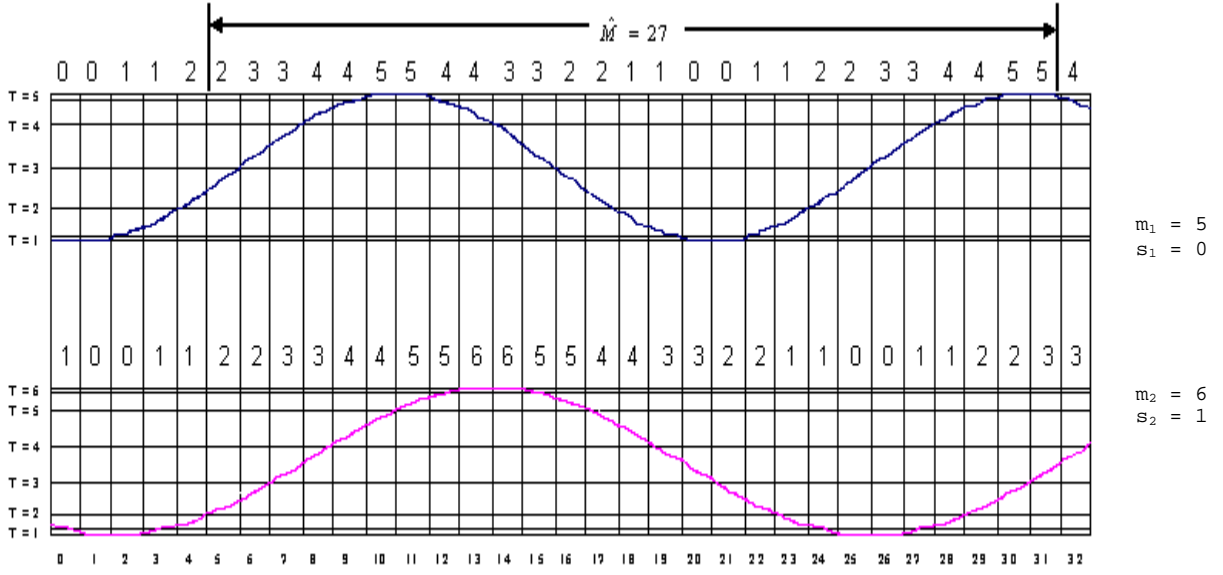


Figure 3.1: Folding Waveforms and Integer Values Within Moduli $m_1 = 5$ and $m_2 = 6$ for the RSNS. [From Ref 4]

The system dynamic range (\hat{M}) of the RSNS is the maximum number of distinct vectors without a redundancy. The selection of the shift and the permutations among the 2 moduli has no effect on \hat{M} . However, the point indices corresponding to \hat{M} (beginning point and ending point) are different. Let m_1 and m_2 be relatively prime integers, $5 \leq m_1 < m_2$. The system dynamic range of the two-channel RSNS with moduli m_1 and m_2 is

$$4m_1 + 2m_2 - 4 \quad (3.7)$$

when $m_2 \leq m_1 + 2$, and

$$4m_1 + 2m_2 - 2 \quad (3.8)$$

when $m_2 \geq m_1 + 3$ [7]. When $m_1=8$ and $m_2=17$, $\hat{M}=64$, which fits equation 3.8.

B. RSNS PROTOTYPE ANTENNA

To demonstrate the efficiency of the RSNS preprocessing, the design of a 6-bit antenna using $m_1 = 8$ and $m_2 = 17$ is considered [3]. A schematic diagram of the RSNS antenna is shown in Figure 3.2 for shifts of $s_1=0$, $s_2=1$ resolution bins.

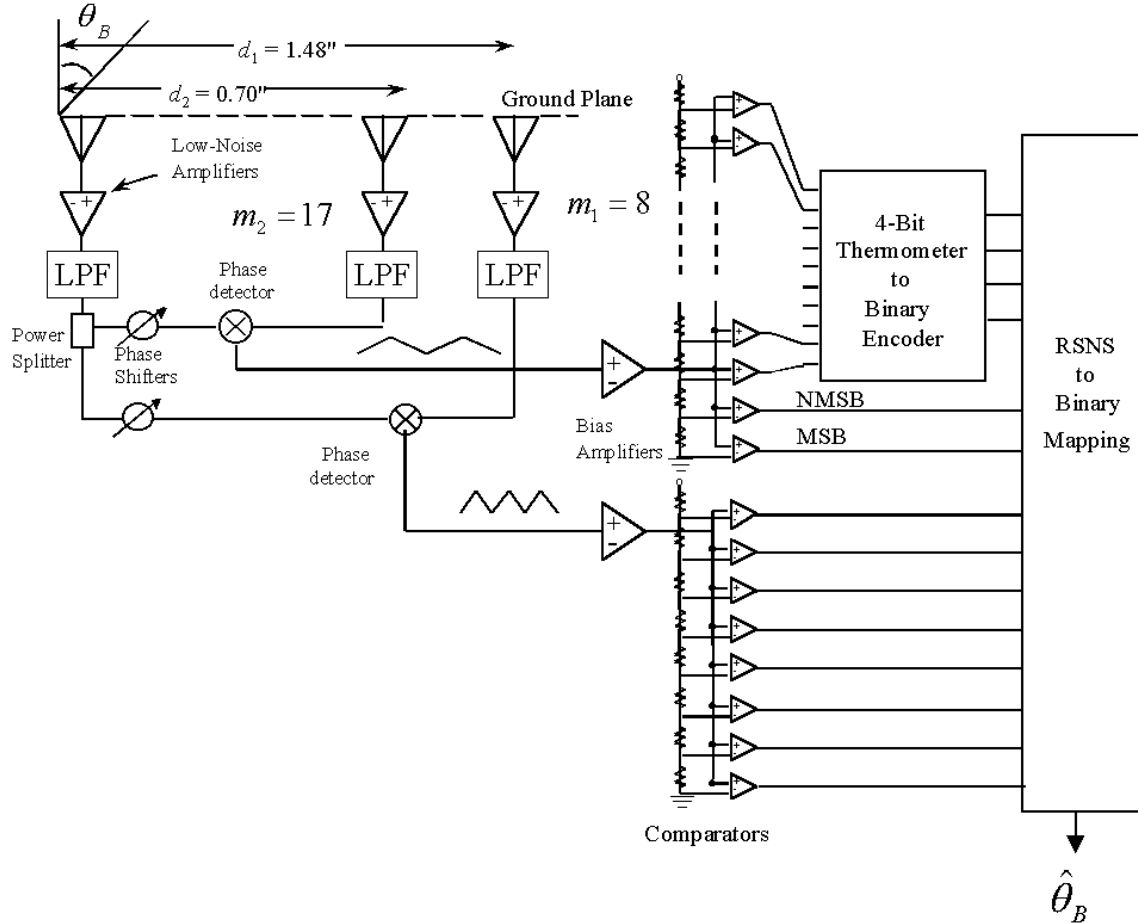


Figure 3.2: Block Diagram of the Unscaled, Original RSNS Antenna System. [From Ref 3]

The number of folds within each modulus is given by

$$n_i = \frac{\hat{M}}{P_{RSNS}} = \frac{\hat{M}}{2m_i N} \quad (3.9)$$

or $n_1=2$ and $n_2=0.94$. The required distance between antenna elements is

$$d_i = n_i \frac{\lambda}{2} = \frac{\hat{M} \lambda \xi}{4m_i N} \quad (3.10)$$

With a scale factor of $\xi=2/\sqrt{3}$, $d_1=1.70$ inches and $d_2=0.80$ inches. For a normalized folding waveform amplitude (-1 to 1), the threshold for the j^{th} comparator for the modulus m_i channel is [6]

$$V_{j,m_i} = \cos \left(\frac{m_i - j + \frac{1}{2}}{m_i} \pi \right) \quad (3.11)$$

The input signal is applied in parallel to both interferometers. The output from each phase detecting mixer is amplitude analyzed using m_i comparators. For this design, there are a total of 25 comparators with a maximum of 17 loaded in parallel. An RSNS-to-binary logic block translates the RSNS residues (number of comparators ON in each thermometer code) to a more convenient representation. The logic block and corresponding bin number are shown in Figure 3.3.

| Vector | Mod 8 | Mod 17 | Bin | Vector | Mod 8 | Mod 17 | Bin | Vector | Mod 8 | Mod 17 | Bin |
|--------|-------|--------|-----|--------|-------|--------|-----|--------|-------|--------|-----|
| 1 | 0 | 0 | | 34 | 1 | 16 | 13 | 67 | 1 | 1 | 46 |
| 2 | 1 | 0 | | 35 | 1 | 17 | 14 | 68 | 2 | 1 | 47 |
| 3 | 1 | 1 | | 36 | 2 | 17 | 15 | 69 | 2 | 0 | 48 |
| 4 | 2 | 1 | | 37 | 2 | 16 | 16 | 70 | 3 | 0 | 49 |
| 5 | 2 | 2 | | 38 | 3 | 16 | 17 | 71 | 3 | 1 | 50 |
| 6 | 3 | 2 | | 39 | 3 | 15 | 18 | 72 | 4 | 1 | 51 |
| 7 | 3 | 3 | | 40 | 4 | 15 | 19 | 73 | 4 | 2 | 52 |
| 8 | 4 | 3 | | 41 | 4 | 14 | 20 | 74 | 5 | 2 | 53 |
| 9 | 4 | 4 | | 42 | 5 | 14 | 21 | 75 | 5 | 3 | 54 |
| 10 | 5 | 4 | | 43 | 5 | 13 | 22 | 76 | 6 | 3 | 55 |
| 11 | 5 | 5 | | 44 | 6 | 13 | 23 | 77 | 6 | 4 | 56 |
| 12 | 6 | 5 | | 45 | 6 | 12 | 24 | 78 | 7 | 4 | 57 |
| 13 | 6 | 6 | | 46 | 7 | 12 | 25 | 79 | 7 | 5 | 58 |
| 14 | 7 | 6 | | 47 | 7 | 11 | 26 | 80 | 8 | 5 | 59 |
| 15 | 7 | 7 | | 48 | 8 | 11 | 27 | 81 | 8 | 6 | 60 |
| 16 | 8 | 7 | | 49 | 8 | 10 | 28 | 82 | 7 | 6 | 61 |
| 17 | 8 | 8 | | 50 | 7 | 10 | 29 | 83 | 7 | 7 | 62 |
| 18 | 7 | 8 | | 51 | 7 | 9 | 30 | 84 | 6 | 7 | 63 |
| 19 | 7 | 9 | | 52 | 6 | 9 | 31 | 85 | 6 | 8 | |
| 20 | 6 | 9 | | 53 | 6 | 8 | 32 | 86 | 5 | 8 | |
| 21 | 6 | 10 | 0 | 54 | 5 | 8 | 33 | 87 | 5 | 9 | |
| 22 | 5 | 10 | 1 | 55 | 5 | 7 | 34 | 88 | 4 | 9 | |
| 23 | 5 | 11 | 2 | 56 | 4 | 7 | 35 | 89 | 4 | 10 | |
| 24 | 4 | 11 | 3 | 57 | 4 | 6 | 36 | 90 | 3 | 10 | |
| 25 | 4 | 12 | 4 | 58 | 3 | 6 | 37 | 91 | 3 | 11 | |
| 26 | 3 | 12 | 5 | 59 | 3 | 5 | 38 | 92 | 2 | 11 | |
| 27 | 3 | 13 | 6 | 60 | 2 | 5 | 39 | 93 | 2 | 12 | |
| 28 | 2 | 13 | 7 | 61 | 2 | 4 | 40 | 94 | 1 | 12 | |
| 29 | 2 | 14 | 8 | 62 | 1 | 4 | 41 | 95 | 1 | 13 | |
| 30 | 1 | 14 | 9 | 63 | 1 | 3 | 42 | 96 | 0 | 13 | |
| 31 | 1 | 15 | 10 | 64 | 0 | 3 | 43 | 96 | 0 | 14 | |
| 32 | 0 | 15 | 11 | 65 | 0 | 2 | 44 | 97 | 1 | 14 | |
| 33 | 0 | 16 | 12 | 66 | 1 | 2 | 45 | 98 | 1 | 15 | |

Figure 3.3: RSNS Logic Block. [From Ref 3]

A consequence of quantizing the angle of arrival into a bin is that the RSNS reports any signal that falls within a bin as if it arrived at the bin center, $\hat{\theta}_k$. This results in a quantization error with a maximum value of half the bin width. The AOA resolution or bin width in θ -space for the k^{th} bin is

$$r_k = \arcsin\left(\frac{2k - \hat{M} + 2}{\xi \hat{M}}\right) - \arcsin\left(\frac{2k - \hat{M}}{\xi \hat{M}}\right) \quad (3.12)$$

Another advantage of the RSNS is that small phase errors can be tolerated without a serious error in the reported AOA due to the inherent Gray Code properties. These phase errors cause the folded waveform from the mixer to shift, thus triggering an incorrect comparator state change. Because the waveforms from the mixers are quantized, the bin width or r_k relaxes the requirements on the antenna circuitry and limits AOA reporting errors to the adjacent quantization levels (bins). However, there is a limit to this feature. If the phase error becomes too great, the comparators will not change state in the correct sequence, which may or may not correspond to a code that is mapped in the dynamic range, \hat{M} . For the system designed, a tolerance study determined that a phase error of 6° is acceptable in the modulus 17 channel and a phase error of 12° in the modulus 8 channel. Figures 3.4, 3.5 and 3.6 show the simulated transfer function. Figure 3.4 is the transfer function with no phase error in both channels. Figures 3.5 and 3.6 are the modulus 8 channel with 0° of phase error and 3° and 6° phase error in the modulus 17 channel. Note how the transfer function becomes jagged and erratic as the phase error is increased until it becomes discontinuous at 6° .

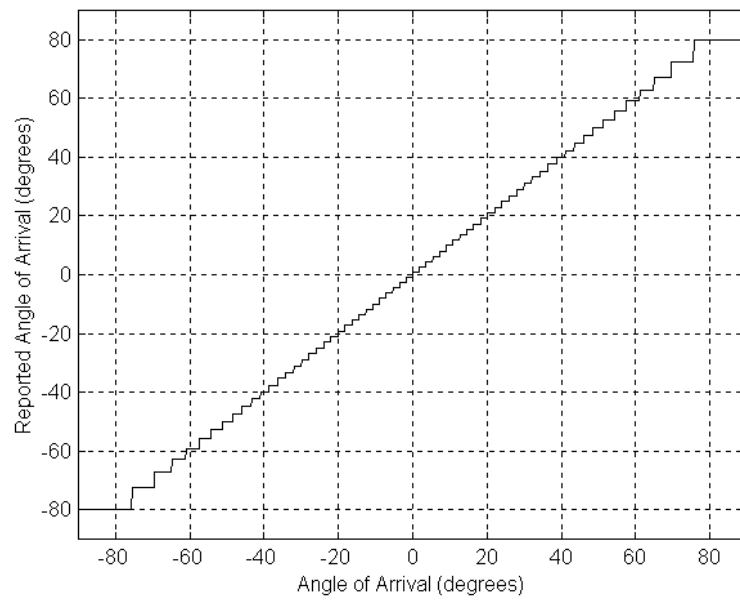


Figure 3.4: Simulated Transfer Function with No Phase Errors in Either Channel. [From Ref 3]

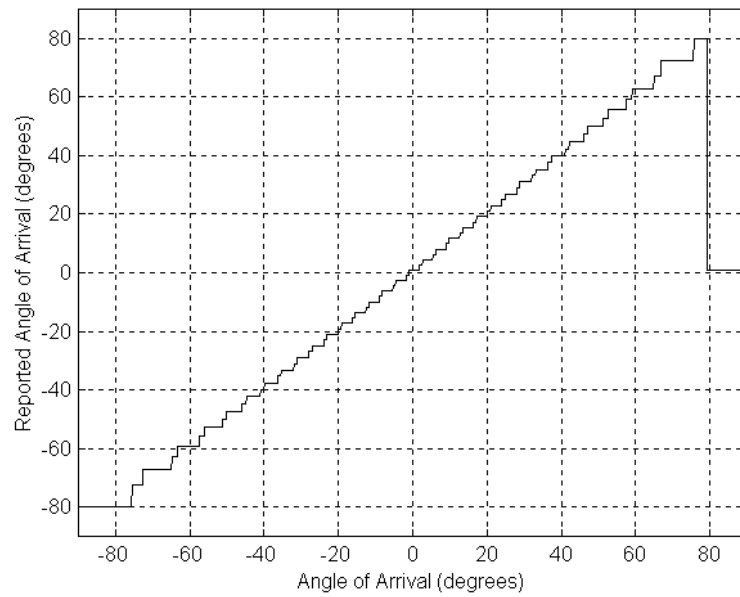


Figure 3.5: Modulus 17 Channel with 3° Phase Error Introduced. [From Ref 3]

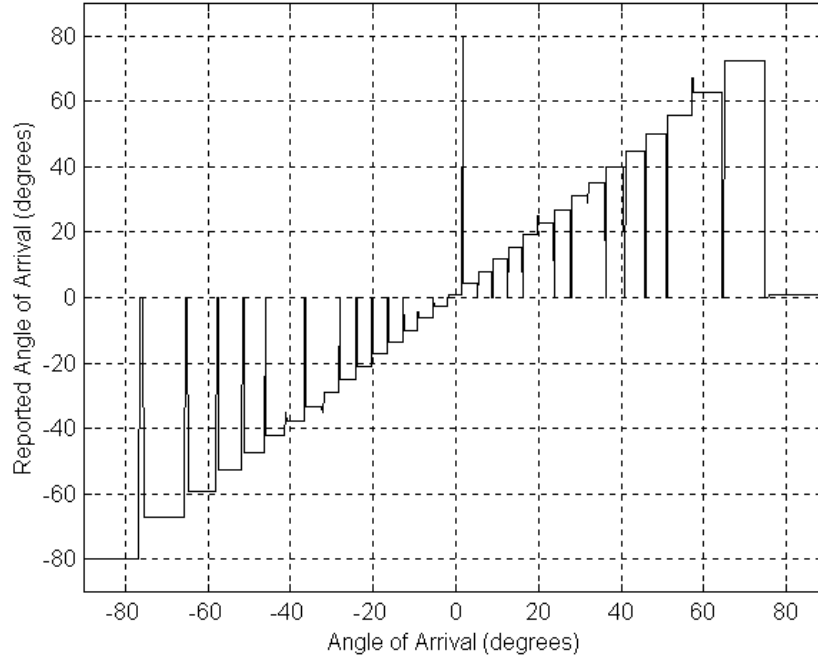


Figure 3.6: Modulus 17 Channel with 6° Phase Error Introduced. [From Ref 3]

C. EXPERIMENTAL RESULTS

An RSNS array based on the moduli $m_1 = 8$ and $m_2 = 17$ was designed, fabricated and tested at a frequency of 8.0 GHz [6]. The schematic diagram of the two-channel array is shown in Figure 3.2. The radiating elements are printed circuit dipoles. For moduli $m_1 = 8$ and $m_2 = 17$, the unscaled distances, $\xi=1$, are $d_1=1.48$ inch and $d_2=0.70$ inch. With $\hat{M}=64$, the number of folding periods $n_1=2$ and $n_2=0.94$. To provide an adequate signal-to-noise ratio, a low-noise amplifier is included at the output of each interferometer element. Also included in the RSNS array is a lowpass filter in each channel to eliminate the amplifier harmonics that are present. Since the common element splits the signal into N paths, an attenuator is placed in the other branches to balance the amplitudes. A fixed phase shifter is also included in one branch of each interferometer so

that the symmetrically folded phase response waveforms from each mixer may be aligned. This alignment ensures that the comparators in the digital processor properly sample the phase waveform and encode it in the RSNS. For the $m_1 = 8$ channel, 8 comparators are required. For the $m_2 = 17$ channel 17 comparators are required. The EEPROM that was used accommodates 15 inputs. The modulus 17 channel processing is conducted in two stages. In the first stage, the 4-bit thermometer to binary encoder maps the 15 least significant codes out of the 17 comparators (ones with the smallest threshold). The remaining two comparators are mapped on the second EEPROM along with the 4 bit binary encoder output and all modulus 8 comparators. The digital processor puts out a bin number k corresponding to the estimated AOA $\hat{\theta}$. The estimated AOA for bin k is given as

$$\hat{\theta}_k = \arcsin \left(\frac{2k+1}{\xi \hat{M}} - \frac{1}{\xi} \right) \quad (3.13)$$

The normalized mixer folding waveform outputs are shown with the simulated waveforms in Figures 3.7 for the $m_1=8$ channel and 3.8 for $m_2=17$ channel for $\xi=1.0$. The basic features correspond to predicted curves. The measured folding outputs from the shift and bias amplifiers in both channels are shown in Figure 3.9. The digital circuit maps the phase difference at the mixer output into an estimated angle of arrival. The predicted output of the unscaled prototype array is reproduced as Figure 3.10. The measured mixer output contains phase errors, which result in differences between the simulated and predicted data. These phase errors cause the thermometer code to

incorrectly map the incident wave to the proper angle of arrival. The measured transfer function of the unscaled prototype antenna is shown in Figure 3.11.

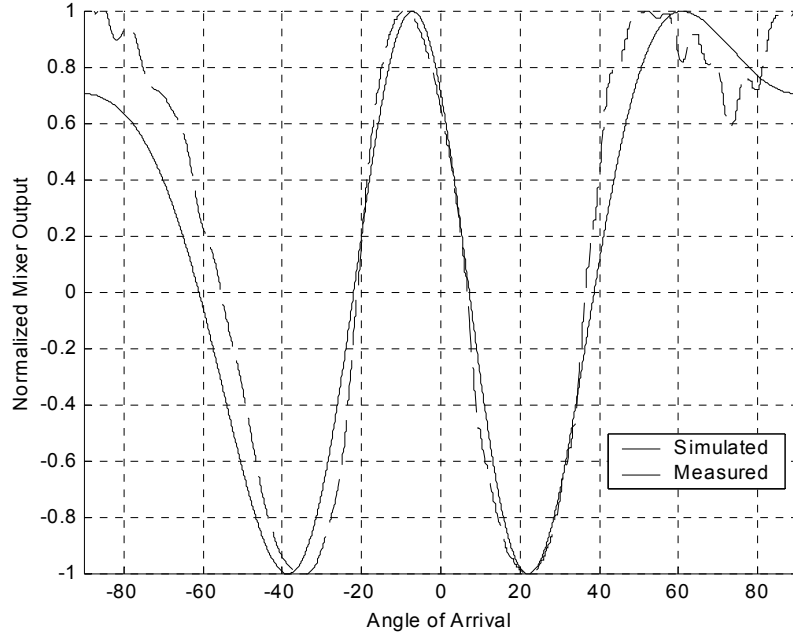


Figure 3.7: Normalized Mixer Output and Simulation Waveforms for RSNS Array with $m_1=8$. [From Ref 3]

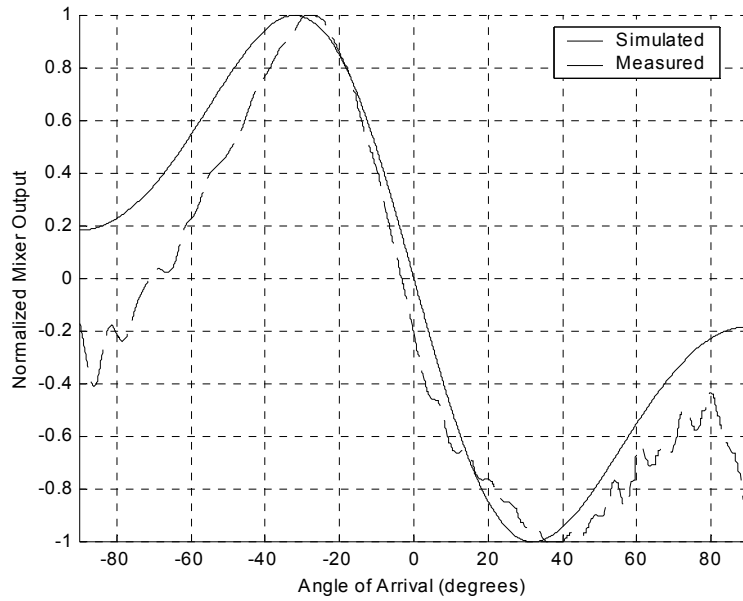


Figure 3.8: Normalized Mixer Output and Simulation Waveforms for RSNS Array with $m_2=17$. [From Ref 3]

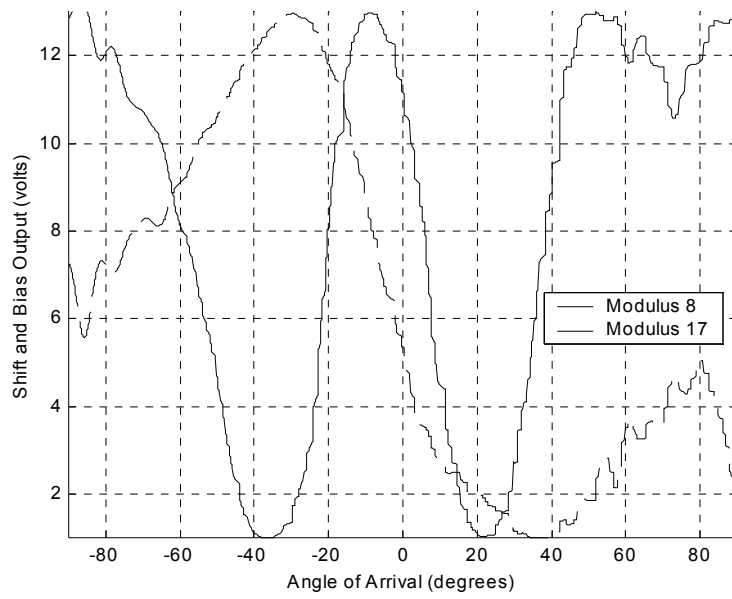


Figure 3.9: Measured Folding Waveform Outputs from the Shift and Bias Amplifiers. [From Ref 3]

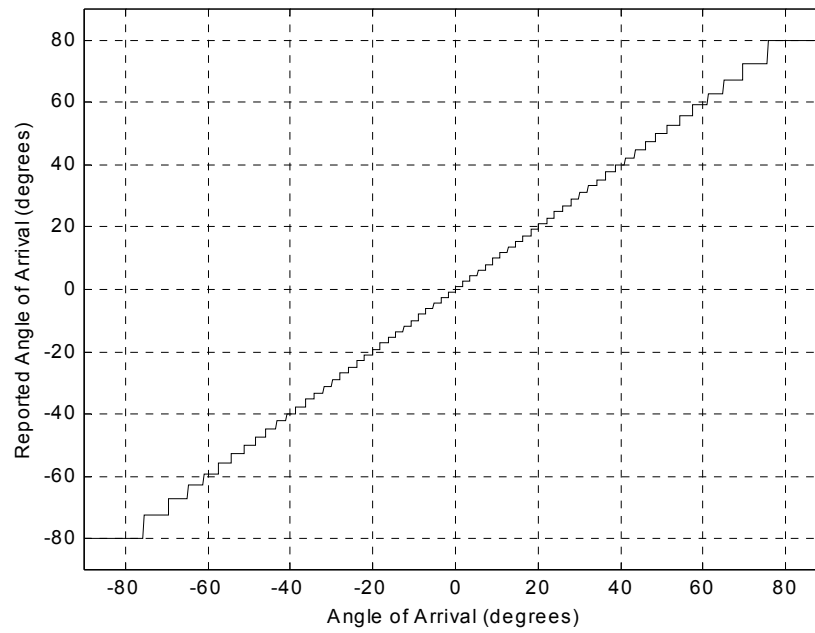


Figure 3.10: Predicted RSNS Transfer Function. [From Ref 3]

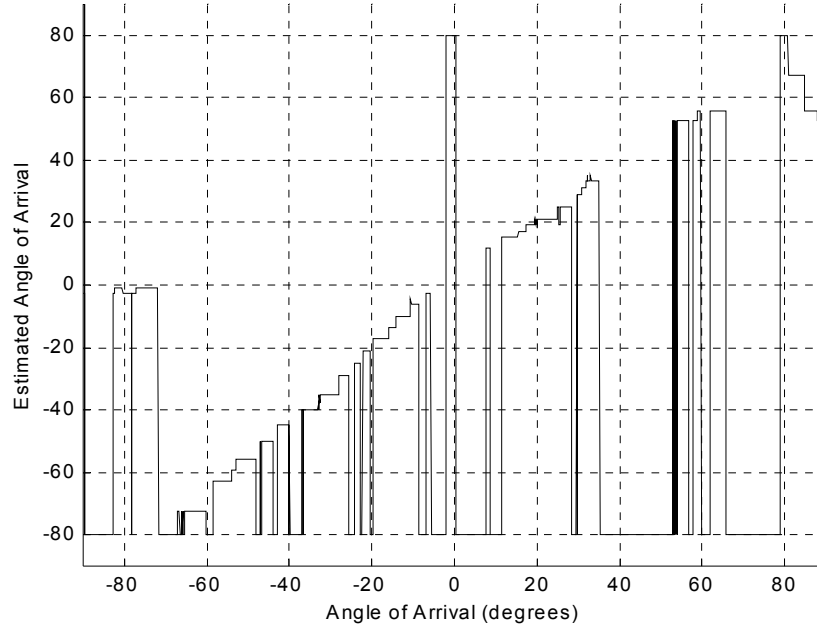


Figure 3.11: Measured RSNS Transfer Function.
[From Ref 3]

The large discontinuities in the transfer function are due to phase and amplitude errors, which arise from several sources. Mutual coupling is a common cause of phase front distortion in small arrays of closely spaced elements. In order to increase the distance between elements and thus reduce the mutual coupling, a scale factor ξ was introduced. The scale factor is the ratio of the element spacings of the unscaled and scaled arrays. Raising the scale factor narrows the mapable FOV of the antenna and increases the resolution within the mapable FOV. For a scale factor of $\xi = 2/\sqrt{3}$, the maximum mapable aperture (θ_{MM}) is $\pm 60^\circ$. The predicted transfer function for the scaled array is shown in Figure 3.12. The corresponding measured transfer function is reproduced as Figure 3.13. The steeper slope of the scaled transfer function is clearly visible when comparing 3.10 and 3.12.

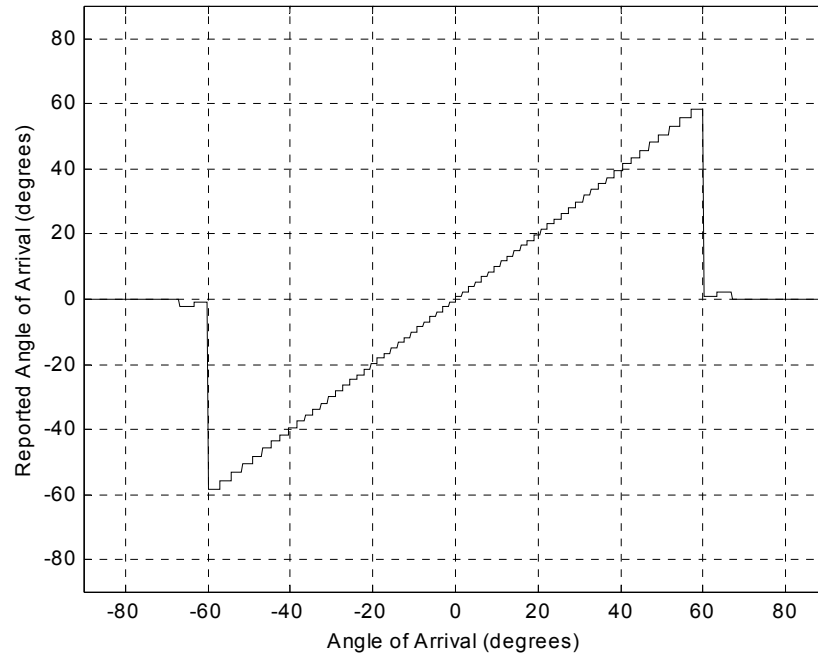


Figure 3.12: Predicted RSNS Transfer Function for Scale Factor $\xi = 2/\sqrt{3}$. [From Ref 3]

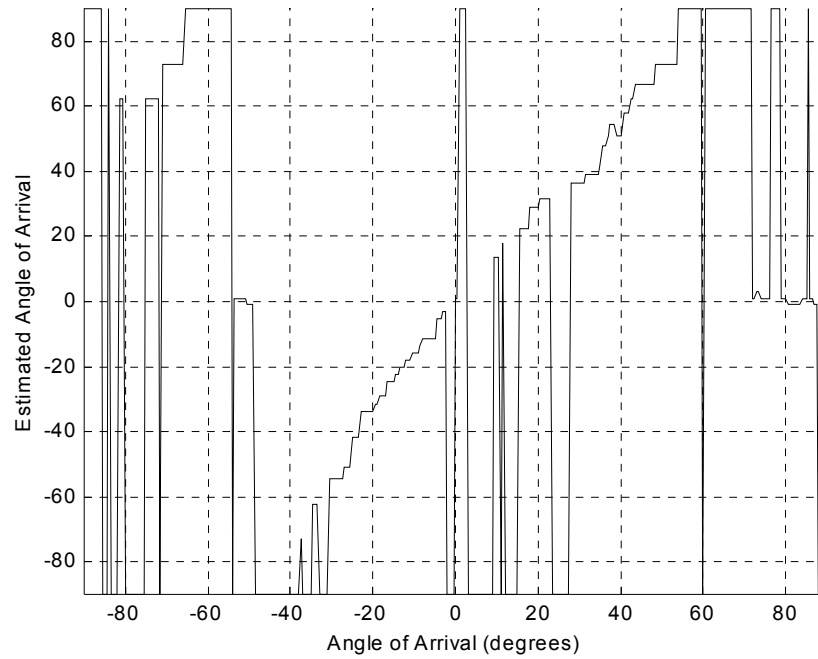


Figure 3.13: Measured RSNS Transfer Function for Scale Factor $\xi = 2/\sqrt{3}$. [From Ref 3]

The transfer function for the scaled array of dipoles does not show any significant improvement due to the reduction of mutual coupling. The microwave circuit has three likely sources of errors: (1) the low noise amplifiers, (2) coaxial cables and phase adjusters, and (3) the rigid connectors. Thus it appears that many small errors accumulate in a manner such that the 6° and 12° error thresholds are exceeded, which results in a degraded transfer function.

D. SECOND GENERATION RSNS ANTENNA

Previous research has introduced the OSNS and the RSNS and showed that they are able to efficiently resolve ambiguities in phase sampling interferometry. The prototype arrays that were built, however, both showed that significant errors are introduced due to the nature of the components and construction of the system. Non-linear components, imperfect devices and mutual coupling are prime contributors to the phase errors present in the folding waveforms. This research took a step forward to validate the RSNS design and to reduce the phase errors in the system.

The Radio Frequency (RF) circuit shown in Figure 3.14 receives a transmitted signal with a set of microstrip antennas (see Figure 3.15). The signal is passed through a set of isolators and then to the first amplification stage. Band-pass filters are used to remove harmonics and the signal is then sent to the second amplification stage. Low-pass filters are used to remove harmonics from the second stage amplifiers. A power splitter is used to divide the reference signal that is passed on to the RF

side of the balanced mixers. The signals from each channel are passed through phase shifters and then to the local oscillator (LO) side of the mixers. Since the frequency at the RF and LO inputs are the same, the mixer output is a DC value that is a function of the AOA. This DC voltage develops a folding waveform as AOA changes. This voltage is amplitude analyzed by the RSNS signal processor in order to estimate the AOA.

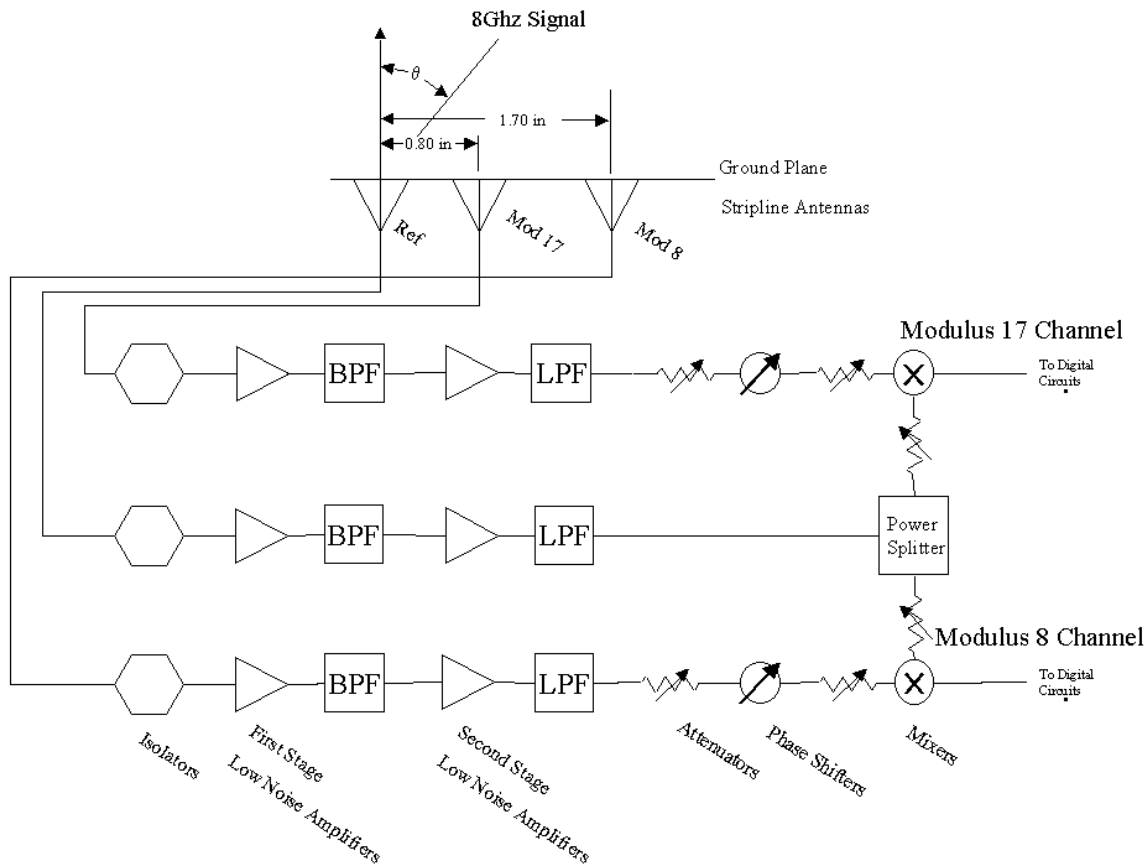


Figure 3.14: RF Circuit Block Diagram. [From Ref 4]

1. Antenna Elements

Since the element spacing for the RSNS array is small, micro-strip antennas were utilized. The microstrip antennas are dipoles designed to resonate at 8.0 GHz. A schematic diagram of a micro-strip dipole antenna is shown

in Figure 3.15. The thickness of each element's substrate is 60 mils (1 mil = .001 inch). The elements are placed into a linear array with the spacings set at 0.80 inch between the reference and modulus 17 element and 1.70 inch between the reference and the modulus 8 element as shown in Figure 3.16. These spacings were chosen over the original design spacings of 0.70 inch and 1.48 inch, since the folding waveform becomes distorted at angles greater than 60° from broadside. By compressing the RSNS dynamic range into the reduced FOV a higher angular resolution is obtained. Antenna pattern measurements were taken of this array one element at a time; both phase and power were recorded. Figures 3.17 and 3.18 show the results respectively.

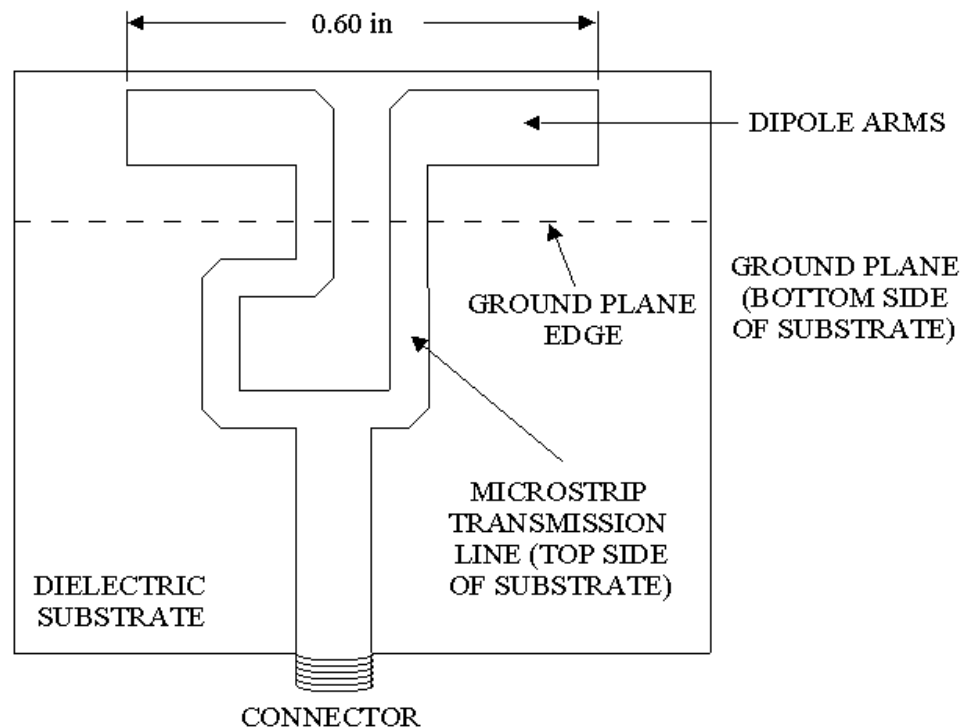


Figure 3.15: Microstrip Dipole Antenna Element.
[From Ref 3]

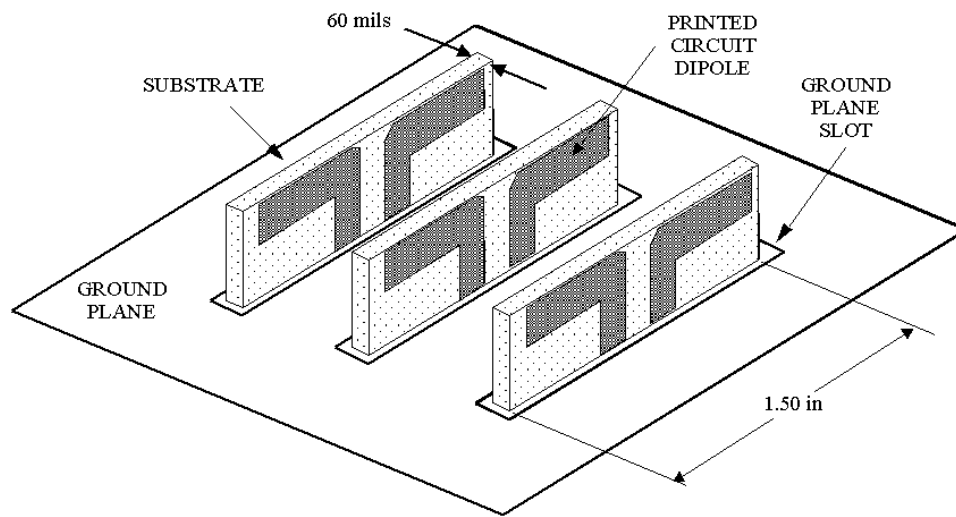


Figure 3.16: Microstrip Antenna Array. [From Ref 3]

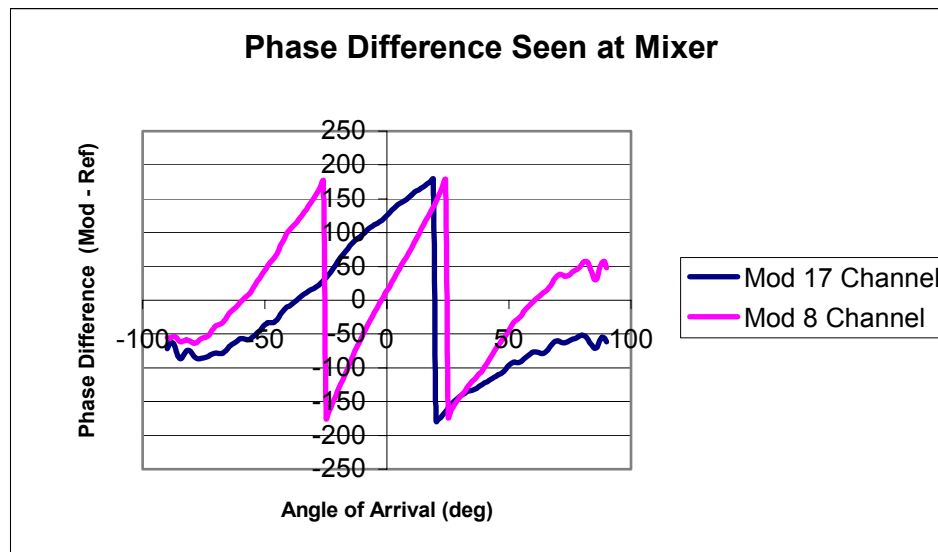


Figure 3.17: Phase Difference Between Modulus and Reference Signals. [From Ref 4]

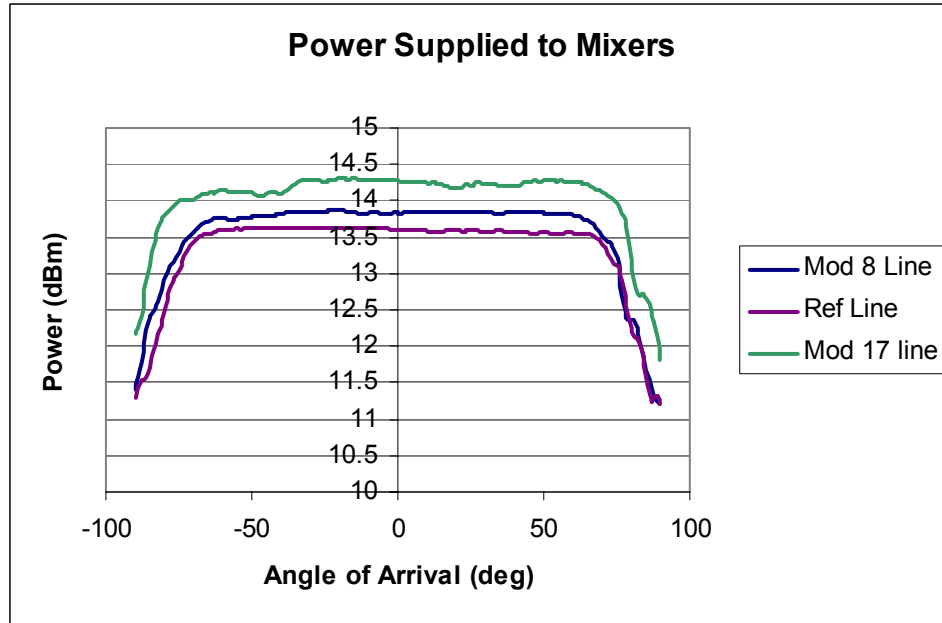


Figure 3.18: Power Measured at the Mixer Inputs.
[From Ref 4]

2. Isolators

M2 Global S70124 isolators were used to further reduce mutual coupling effects and reflections in the feed lines. They are placed between the antenna elements and the first amplification stage. The specifications for the isolators are shown in Table 3.1. After testing the isolators on the network analyzer they were found to meet all the specifications that were supplied.

| Frequency Range (GHz) | Isolation (dB) Minimum | Insertion Loss (dB) Maximum | VSWR Maximum | Temperature Range (°C) | Connector Available | Package Size (in) |
|-----------------------|------------------------|-----------------------------|--------------|------------------------|---------------------|-------------------|
| 7.0 – 12.4 | 20 | 0.5 | 1.25 | -20 to +60 | SMA | .75 x .90 x .50 |

Table 3.1: Isolator Specifications. [From Ref 4]

3. Amplifiers

The system was originally designed with only one stage of amplifiers. A single stage amplifier design was introduced to try and eliminate sources of phase errors that were present in the first prototype. The DBS DWT 18636 amplifiers were used. The goal of the amplification stage is to gain a constant power output independent of AOA at the input of the mixers since any imbalance in power at the mixer inputs will produce phase errors. These microwave amplifiers have two operating regions: linear and saturation. The preferred region for this system is the saturated region. By operating in saturation, the output power of the amplifiers is independent of the input power. Figure 3.19 shows the power curves for the DBS amplifiers.

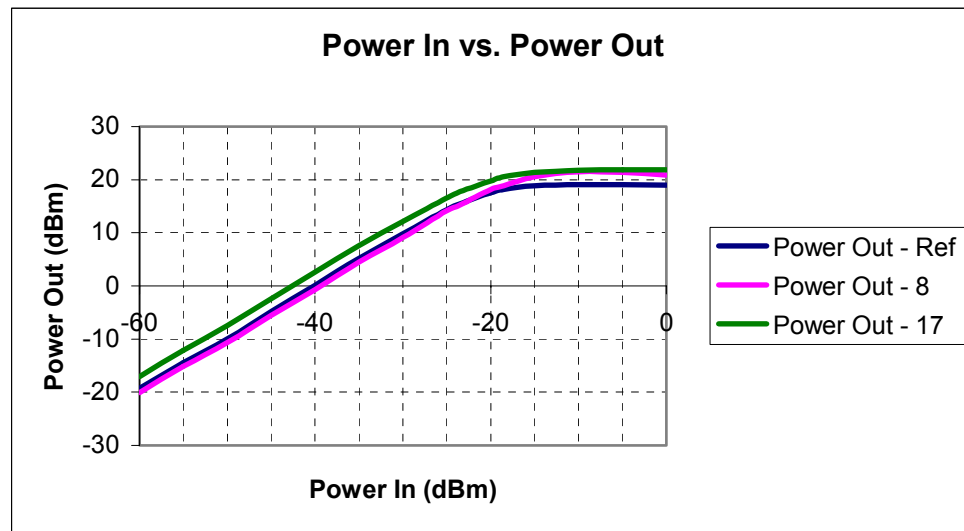


Figure 3.19: Power Curves for DBS Amplifiers.
[From Ref 4]

In order for the system to work well the input power needs to be at least -15 dBm. The initial transmitter

distance was 19 feet. The input power for the amplifiers at this distance was not enough to drive the amplifiers into saturation. A mount was constructed to move the transmitter closer to the antenna elements. However, even with the transmitter at 6' from the elements, the power input to the amplifiers was only -17 dBm. This level was barely enough to saturate the amplifiers, so a two-stage amplifier design was utilized.

The DBS amplifiers are used in the second stage of amplification because the power output levels are well matched and the three were phase matched to within 10°. However, the phase matching was done in the linear region (at low power) and the phase performance of the amplifiers in the saturation region is not known precisely. The first stage amplifiers were chosen based on their power curves. The two primary considerations were maximum gain and how well the power curves matched. Figure 3.20 shows the power curves for the three Avantek amplifiers that were chosen.

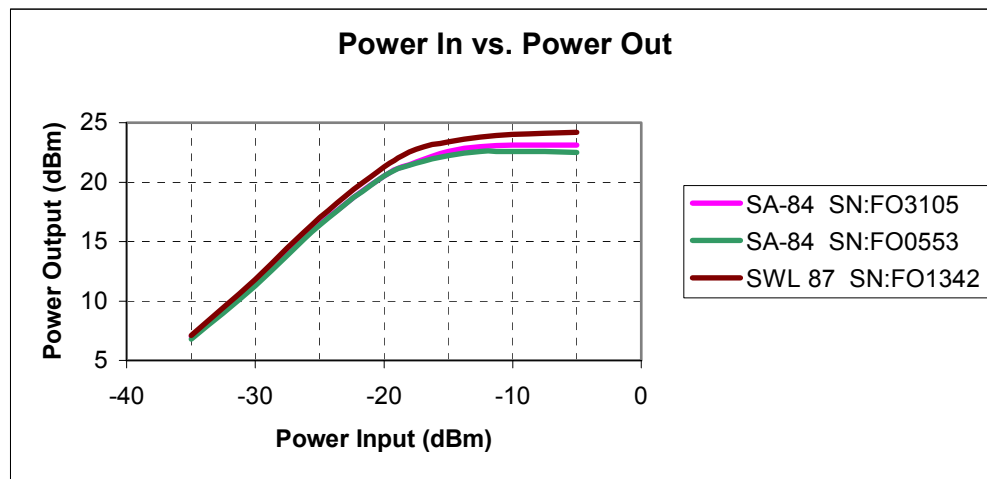


Figure 3.20: Power Curves for Avantek Amplifiers.
[From Ref 4]

Phase matching for this amplification stage is not as important as the second stage. The purpose for the first stage is to drive the second stage amplifiers into saturation. The gain for these amplifiers is approximately 40 dB in the linear region, which is more than enough to saturate the second stage amplifiers at a received power of -50 dBm. The overall effect of the two stages is that the signal output from the second amplification stage remains a constant regardless of the received power by the antenna elements.

4. Filters

The amplifiers used in this system produce harmonics. The harmonic levels are 20 dB lower than the fundamental, but introduce phase errors in the system in excess of 20°. In order to eliminate these errors, filters are used after each stage of amplification. AIRTRON band-pass filters, with a pass band of 4-8 GHz, are used after the first stage amplifiers and MICROLAB/FXR LA-90N low-pass filters are used after the second stage amplifiers. Each filter has an attenuation of 55 dB or greater in the stopband, which effectively eliminates all signals except the fundamental.

5. Mixers

A mixer is a common microwave component that is normally used to translate a higher RF carrier to an intermediate frequency (IF). Typically, the RF signal is combined with a second signal, referred to as the local oscillator (LO), at a non-linear diode. The resulting IF is approximated by $\omega_f = |\omega_f - \omega_o|$ [8]. The $\omega_f + \omega_o$ and other product terms that are generated in the mixer are removed

by filtering. For the RSNS antenna, the mixers are used as phase detectors. The RF and LO inputs are the same frequency, therefore, the IF output is a DC value of

$$\begin{aligned} V_{IF} = & A_1 \cos\left[(\omega_{lo} - \omega_{rf})t - (\phi_{lo} - \phi_{rf})\right] \\ & + A_2 \cos\left[(\omega_{lo} + \omega_{rf})t - (\phi_{lo} - \phi_{rf})\right] \\ & + [\text{higher frequency terms}] \end{aligned} \quad (3.14)$$

Since $\omega_{rf} = \omega_{lo}$,

$$\begin{aligned} V_{IF} = & A_1 \cos(\phi_{rf} - \phi_{lo}) + A_2 \cos(2\omega t) \\ & + (\text{higher frequency terms}) \end{aligned} \quad (3.15)$$

With proper filtering the $2\omega t$ and higher frequency terms can be eliminated. The remaining DC term depends solely on the phase difference $(\phi_{rf} - \phi_{lo})$,

$$V_{IF} = A_1 \cos(\phi_{rf} - \phi_{lo}) \quad (3.16)$$

The Anaren 70540 balanced mixer was selected due to its superior phase response as seen on the network analyzer. For this application, the important specification is the IF frequency range. By having the range set below 2ω , it effectively filters the output of the mixer. Figure 3.21 shows the first set of folding waveforms with the power level to the inputs at 14 dBm. The maximum and minimum regions of the folding waveforms appear to be flattened, indicating that the mixer is

saturating. Attenuators were added at the mixer inputs until the regions regained their predicted shape.

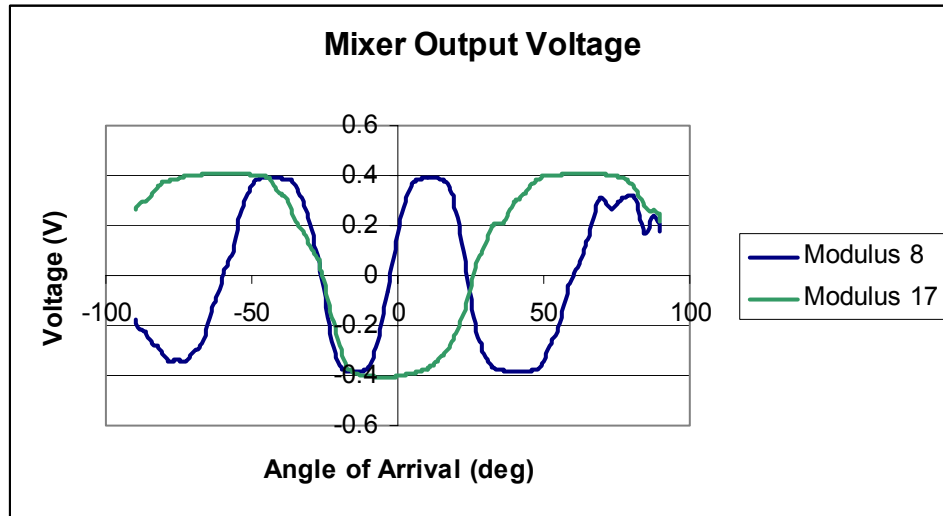


Figure 3.21: Folding Waveforms from Saturated Mixers.
[From Ref 4]

6. Miscellaneous Components

The phase difference between the reference signal and the channel signal is the basis for AOA estimations. The phase difference at broadside defines a convenient relationship between the folding waveforms and can be used for calibration of the antenna hardware. In order to set the phase angles in each of the channels, the lengths of the semi-rigid coaxial cable were precisely cut. Because predicting how the phase of the signal is affected by the amplifiers and other components is difficult, phase adjusters were added. The phase adjusters are variable length coaxial cables that contain no dielectric medium. At 8.0 GHz, one turn of the barrel will change the phase of the signal by 5° giving the phase adjuster a range of approximately 60° .

Attenuators are also added to each signal line. The purpose of the first set of attenuators is to balance the power between the reference signal and the modulus signal at the output of the second amplification stage. A second set of attenuators is added to reduce the power input to the mixers, since the 20 dBm output of the second stage amplifiers saturates the mixers, causing phase errors.

7. Structural Design

The system is assembled on a $\frac{1}{4}$ inch brass plate measuring 13 inches by 13 inches. The plate serves two purposes. The first is structural: by attaching the components to the plate any vibrational errors that might be introduced are eliminated. The second function of the brass plate is as a heat sink. The amplifiers will operate at a high temperature, which may introduce phase errors into the system. The brass plate keeps the entire system at a constant temperature that is only slightly above room temperature, thus minimizing errors. All coaxial cables are cut to length. These custom fit lines minimize bends in the cables and the number of connectors that are needed to assemble the system.

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IV. IMPROVED ROBUST SYMMETRICAL NUMBER SYSTEM SIGNAL PROCESSING CIRCUIT

A. OVERVIEW

The RSNS Signal Processing Circuit transforms the two DC signals coming from the antenna into a binary output corresponding to the RSNS bin number of the incident wave direction and ultimately to a digital readout displaying the estimated AOA. After the signals leave the mixers as shown in Figure 4.1, transformation begins with amplification and biasing of the detected phase signals. The phase signals are supplied to independent comparator ladders that amplitude analyze the signal in a thermometer code. The comparators supply their outputs to a latch for digital processing.

Digital processing begins with determination of the level of each analog signal in the 1-of-N circuitry. At this point, with a single logic gate representing the level of each modulus, the combinations of moduli levels that exist within the system's dynamic range are paired in the notional Bin Mapping AND field. The logical output of this pairing is then mapped to a binary number corresponding to the RSNS bin number. This six bit binary number is then passed to an output latch to provide a clean transition between output states. The output latch provides this binary signal to any automated display, notification and/or tracking system for processing necessary to meet the ultimate application's needs. A digital readout is implemented here with the binary output also supplied to a PC for development of the system's transfer function.

The description that follows only discusses the

details of the modulus 8 portion of the circuit, but modulus 17 portions are similarly constructed. Specific binary values presented in the figures correspond to Bin 57 values for illustrative purposes.

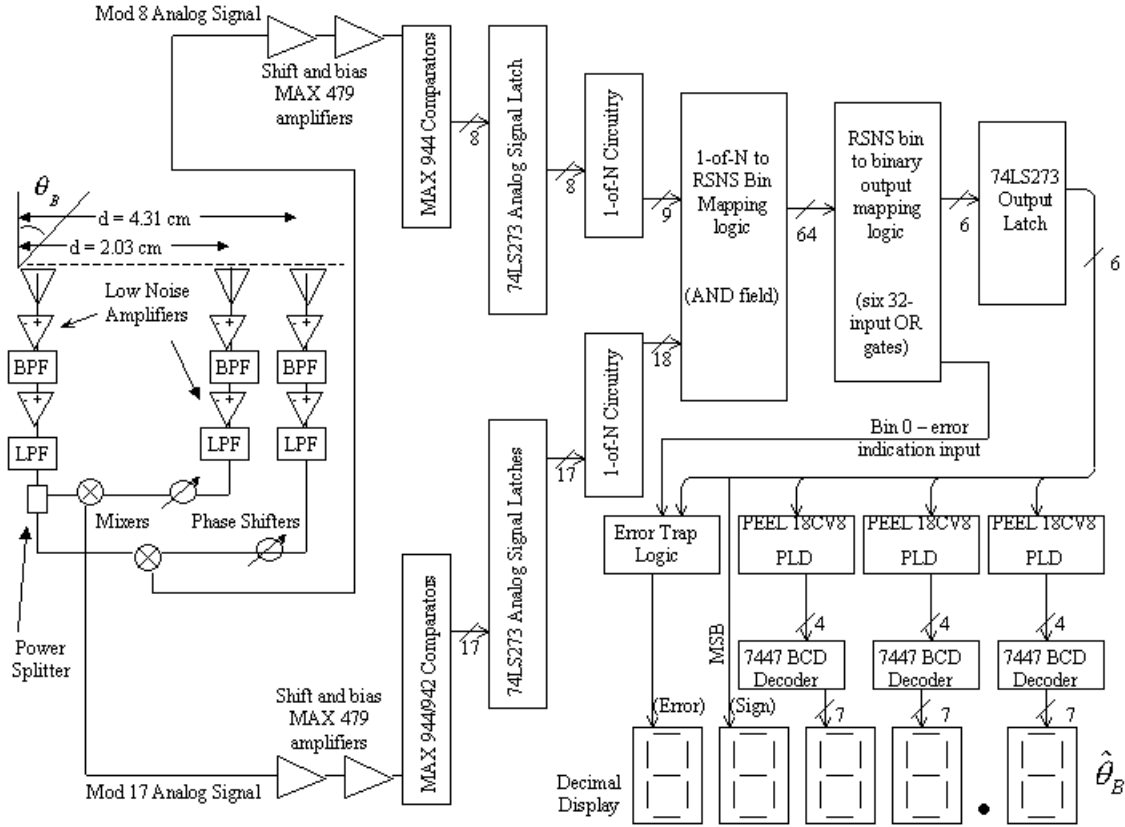


Figure 4.1: RSNS DF System Block Diagram.

B. SHIFT AND BIAS AMPLIFIERS

The first component encountered in the RSNS processing circuit is an inverting amplifier. As illustrated in Figure 4.2, this MAX 479 operational amplifier multiplies the nominally ± 320 mVdc signal from the antenna by a factor initially set at seven. This amplification is necessary to provide margins between each successive threshold level to encompass comparator resolution margin plus a necessary hysteresis value. Adjustment of the amplification

multiplier can be accomplished by the potentiometer identified in Figure 4.2 as R1 in the feedback loop of each amplifier. Adjustment may be necessary to compensate for any variation in the antenna's response. The second component encountered in the signal path is a second MAX 479, serving as an inverting operational amplifier to shift the signal to center around 2.5 Vdc. This shift is performed to preclude the necessity of using dual power supplies in the comparator ladder section of the processor. This shifting can be altered by adjustment of the potentiometer in the shift amplifier's voltage divider identified as R2 in Figure 4.2. The MAX 479 Quad Micropower, Single-Supply, Operational Amplifier chip from Maxim Integrated Products was selected for this application and contains four amplifiers on a single chip versus the previously used LM741 with one amplifier per chip, thus significantly reducing the footprint of this stage.

The voltage divider for the shift amplifiers is powered by a MAX 675 voltage reference chip from Maxim Integrated Products. This design was implemented versus using the same power as that which supplies VCC due to the fairly small margins between threshold levels and the deleterious effects a wavering or even minimally misadjusted supply would have on the comparison process in the following stage. The MAX 675 controls its 5 Vdc output within a 2.5 mVdc range when supplied with 15 Vdc.

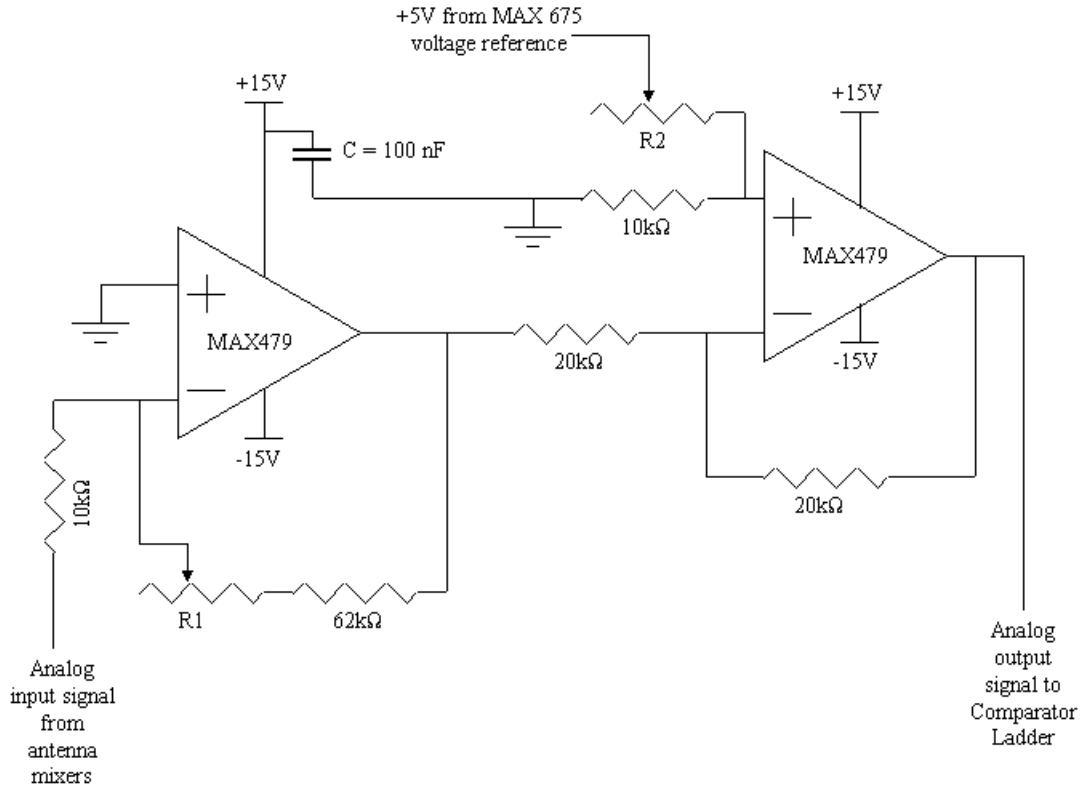


Figure 4.2: Shift and Bias Amplifiers.

C. COMPARATOR LADDER

A comparator ladder follows shifting and amplification as the first step in determining the quantized voltage level. This is shown in Figure 4.3 and accomplished by supplying each analog signal to a parallel grouping of comparators (8 for modulus 8 and 17 for modulus 17) which are also supplied with a reference voltage representing RSNS threshold levels. These reference voltages are computed per equation 3.11 and shown on Table 4.1. Each comparator will shift its output to the positive rail value (+5 Vdc here to simplify TTL implementation) when its signal exceeds its reference plus a 1 mVdc hysteresis margin. Conversely, when the signal lowers to a 1 mVdc hysteresis margin below the reference voltage, the

comparator will shift its output to the comparator's negative rail, implemented as circuit ground.

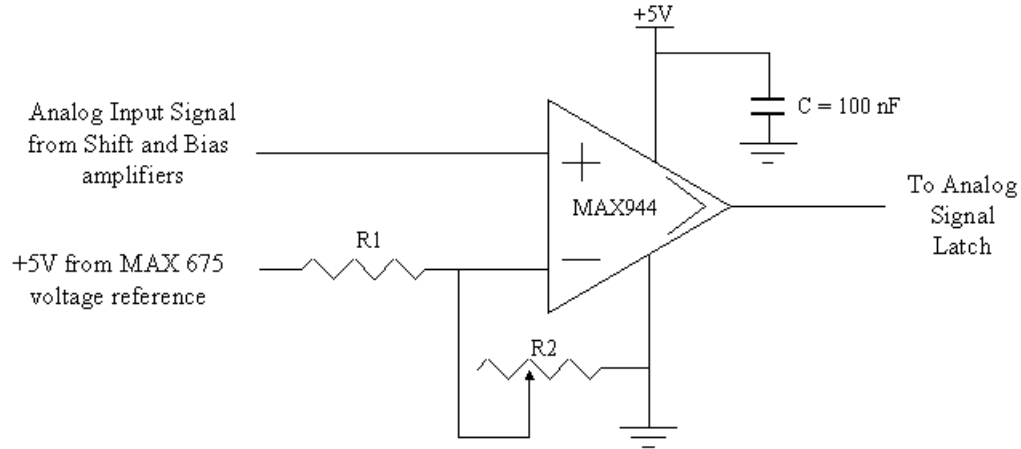


Figure 4.3: Comparator Circuit.

Reference voltage implementation is accomplished by a voltage divider at each comparator supplied by a common MAX 675 voltage reference identical to the one used in the shift and bias amplification stage. The comparators have a maximum input offset current of 100 nA. Making the offset current have a negligible effect on the voltage divider calculations (less than 1% of total current) requires passing at least 10 micro-amps through the voltage divider, thus necessitating a maximum resistance of 500k ohms. The MAX 675 will supply a maximum load current of 30 mA when supplied at 15 Vdc, therefore requiring a combined load resistance of at least 167 ohms. A standard value of 2.4k ohms was selected for R1 and a potentiometer of appropriate range was selected as R2 (see Table 4.1). Load current from the MAX 675 is calculated to be at 26 mA, well within the specification. Selection of potentiometer range included ensuring the initial setting was within 10 to 90% of full range to allow for adjustability in the occurrence of circuit or waveform changes.

| | Volts | R1 value Ω | R2 value Ω | R2 range Ω |
|---------------|--------|-------------------|-------------------|-------------------|
| Mod 8 | | | | |
| Comparator 1 | 0.303 | 2400 | 154.8 | 1000 |
| Comparator 2 | 0.638 | 2400 | 351.0 | 1000 |
| Comparator 3 | 1.256 | 2400 | 805.1 | 1000 |
| Comparator 4 | 2.063 | 2400 | 1685.8 | 10000 |
| Comparator 5 | 2.937 | 2400 | 3416.8 | 10000 |
| Comparator 6 | 3.744 | 2400 | 7154.1 | 10000 |
| Comparator 7 | 4.362 | 2400 | 16408.8 | 20000 |
| Comparator 8 | 4.697 | 2400 | 37204.0 | 50000 |
| Mod 17 | | | | |
| Comparator 1 | 0.2696 | 2400 | 136.8 | 1000 |
| Comparator 2 | 0.3455 | 2400 | 178.2 | 1000 |
| Comparator 3 | 0.4948 | 2400 | 263.6 | 1000 |
| Comparator 4 | 0.7124 | 2400 | 398.8 | 1000 |
| Comparator 5 | 0.9909 | 2400 | 593.2 | 1000 |
| Comparator 6 | 1.321 | 2400 | 861.8 | 1000 |
| Comparator 7 | 1.691 | 2400 | 1226.5 | 10000 |
| Comparator 8 | 2.088 | 2400 | 1720.9 | 10000 |
| Comparator 9 | 2.5 | 2400 | 2400.0 | 10000 |
| Comparator 10 | 2.912 | 2400 | 3347.1 | 10000 |
| Comparator 11 | 3.309 | 2400 | 4696.4 | 10000 |
| Comparator 12 | 3.679 | 2400 | 6684.0 | 10000 |
| Comparator 13 | 4.009 | 2400 | 9709.0 | 50000 |
| Comparator 14 | 4.288 | 2400 | 14453.9 | 50000 |
| Comparator 15 | 4.505 | 2400 | 21842.4 | 50000 |
| Comparator 16 | 4.654 | 2400 | 32282.1 | 50000 |
| Comparator 17 | 4.73 | 2400 | 42044.4 | 50000 |

Table 4.1: Comparator Ladder Voltage Divider values.

The MAX 944 and MAX 942 High-Speed, Low-Power, 3V/5V, Rail-to-Rail, Single-Supply Comparators from Maxim Integrated Products were selected for this application. The MAX 944 has four comparators per DIP14 chip and the MAX 942 has two comparators per DIP8 chip. This significantly reduces the footprint over the previously-utilized LM311 with one comparator per chip. The MAX 942 was used for the 25th comparator to further reduce circuit footprint as only one additional comparator was needed. The MAX 941 is the one comparator per DIP8 chip model of this family and was not utilized for the 25th comparator due to the presence of additional features unnecessary for this design. The selected chips have implemented an internal pull-up to the positive rail in addition to an internal hysteresis range of 2 mVdc, thus eliminating the need to externally build these desirable features into the circuit [9]. This further reduces the circuit's footprint and contributed to their selection for this application.

The selected comparators advertise the ability to operate from rail to rail (0 to 5 Vdc in this design), but the implemented range is from 0.26 to 4.74 Vdc to provide a margin of error. This margin could be reduced as desired with adjustment of amplification and threshold adjustment potentiometers. Reduction of this margin may become desirable to expand the gap between successive RSNS levels. The voltage range was selected to allow for seamless integration with the TTL latches and follow-on combinational logic. A 100 nF decoupling capacitor is placed close to the V+ terminal of each comparator chip for improved noise immunity.

D. ANALOG SIGNAL LATCHES

Storing the output of the comparators for digital processing is the job of the analog signal latches. These SN74LS273 Octal D-type Flip-Flop latches from Texas Instruments provide a solid input for the digital logic components that follow, thus eliminating the effects of comparator oscillation caused by a modulus signal close to the RSNS threshold voltage level and changing in excess of the hysteresis value. These latches are placed physically close to, and approximately equidistant from, the comparators to minimize possible propagation time-induced errors.

E. LATCH TIMER

An ICM7555 timer is utilized to provide the clock signal for all latches. The ICM7555 has two astable circuit configurations, with the configuration detailed in Figure 4.4 yielding a 50% duty cycle output using one timing resistor and capacitor.

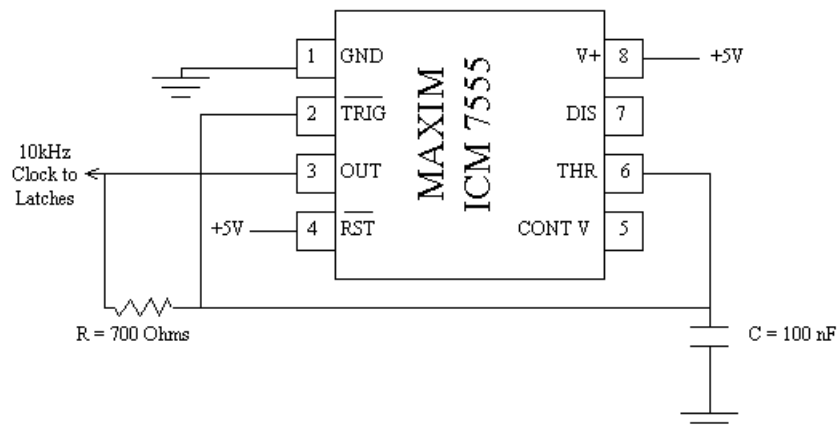


Figure 4.4: Clock Source.

Clock speed determining factors include propagation delay through the digital logic, maximum speed of components and expected rate of change of incoming information. The oscillation frequency is defined by

$$f_c = \frac{1}{1.4RC} \quad (4.1)$$

Table 4.2 shows the maximum propagation delay times for each logic device in the digital processing signal path, plus the times necessary to propagate through the analog signal latch and time necessary to hold a signal constant (at the Output Latch input) before it is guaranteed to be recognized at the next clock cycle.

| Component | Component Delay (ns) |
|--|----------------------|
| SN74LS273 latch (propagation) | 27 |
| DM74LS04 Inverter gate | 15 |
| DM74LS11 3-AND gate | 18 |
| DM74LS00 2-NAND gate | 15 |
| DM74LS30 8-NAND gate | 20 |
| DM74LS32 2-OR gate (2 times) | 15 each |
| SN74LS273 latch (data hold) | 5 |
| TOTAL MAXIMUM PROPAGATION DELAY | 130 |

Table 4.2: Propagation Delay Determination.

The sum total of all delays is shown to be 130ns. This delay mandates that the clock frequency must be less than 7.7MHz to allow sufficient time for the worst case propagation to occur from the analog signal latch to the Output Latch. The ICM7555 has a maximum guaranteed oscillation frequency of 500 kHz, therefore imposing a more

limiting maximum clock speed. The Delay-type flip flops that make up the 74LS273 latch have a maximum clock frequency of 30MHz. This parameter imposes no limitations on the circuit, but needed to be considered for completeness. The expected rate of change of the incoming information will determine the minimum clock frequency and is an operational parameter dependent upon the targets the system is ultimately designed for. This will need to be evaluated fully when those targets are identified. The parameter used for developing a minimum clock frequency in this thesis was the rate of change of simulation inputs as the testing to be done in the anechoic chamber on the antenna assembly is done statically. The initial clock frequency chosen was 1kHz, but caused gaps in the system's transfer function. This will be fully explained in Section V of this thesis. A clock speed of 10kHz was evaluated to be more than adequate to preclude developing the aforementioned gaps in the transfer function. This frequency was selected somewhat arbitrarily, but it satisfies all requirements and was verified to be adequate through extensive simulation.

F. ONE-OF-N DETECTOR

Deciphering the level each modulus presently occupies is the function of the 1-of-N Detector. This portion of the processor (seen in Figure 4.5) accepts its inputs from the analog signal latches and produces a single active logic gate per modulus corresponding to the modulus level. This approach allows the use of discrete logic gates in the following stage versus attempting to decipher 25 inputs simultaneously with a collection of EEPROMs that

necessitate complex electronic overhead and multiple passes through one EEPROM due to the lack of a readily available EEPROM with 25 inputs.

As the level of the modulus rises from its minimum point below the threshold voltage of the comparator supplying latch 1 in Figure 4.5, successive comparators actuate and pass a logical one through the analog signal latch to the input of the 1-of-N Detector. As the thermometer code rises, the 3-input AND gates are activated sequentially due to the presence of a logical one on the non-inverted input and a logic zero on the inverted inputs. The non-inverted inputs correspond to the level which the AND gate is designed to identify as the present modulus level. The inverted inputs correspond to modulus levels above which the AND gate is designed to identify, and provide the information required to uniquely identify where the current modulus level. The lowest and highest levels of each modulus are implemented with a simple configuration of an inverted level 1 latch output (for level 0) and a direct readout of the highest latch level.

A 2-input AND gate would be sufficient to adequately identify the modulus level, but the current design utilizes the 3-input AND gate of the DM74LS11 Triple 3-input AND Gate chip from Fairchild Semiconductors to compensate for a phenomenon known as a sparkle [8]. This phenomenon considers either a faulty comparator or two adjacent comparators with sufficient differences (such as a timing mismatch) that causes them to provide a faulty thermometer code with a changing input signal. A logical zero internal to the rising thermometer code such as the one seen at 2Q of Figure 4.5 is called a sparkle and generates problems in

the binary decoding of the system. The parallel arrangement of digital logic gates at the latch outputs generates a true 1-of-N code in the presence of a single sparkle. This arrangement could be expanded to compensate for more such phenomenon occurrences if desired.

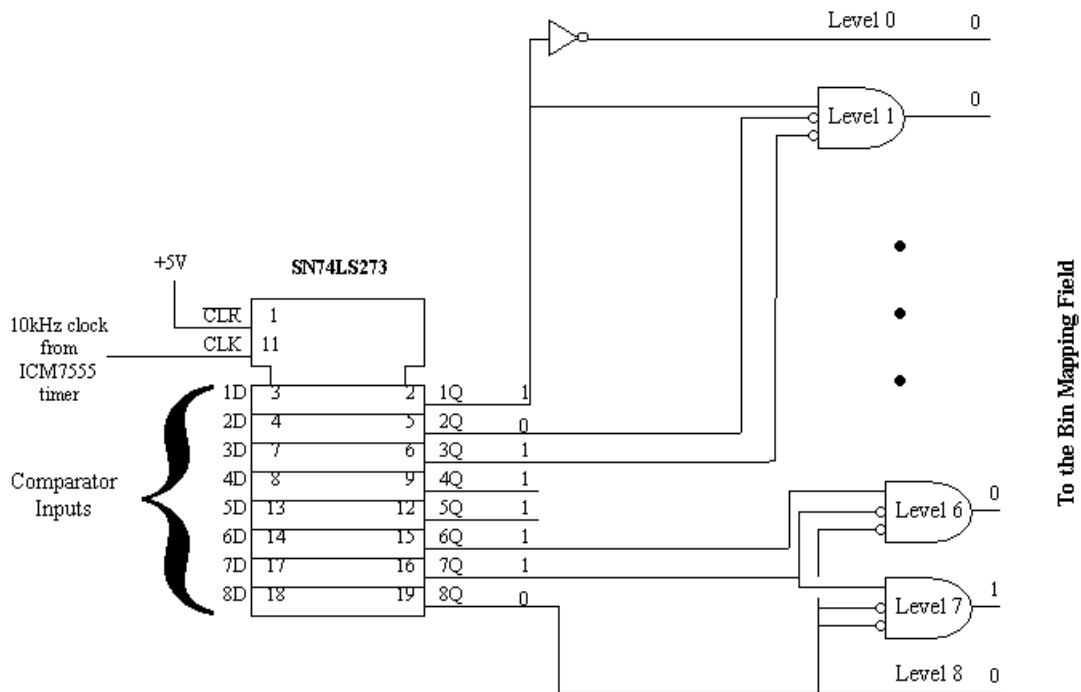


Figure 4.5: Analog Signal Latch and 1-of-N Circuitry.

G. BIN MAPPING FIELD

The Bin Mapping Field pairs all available combinations of the two moduli levels to determine in which RSNS bin the incoming signal resides. This would intuitively be implemented with 64 AND gates, but ultimately takes advantage of NAND-NAND relationships with the Digital Mapping portion of the processor and is implemented with the 74LS00 Quad 2-Input NAND Gate chip. This

implementation is shown in Figure 4.6. Each 2-input NAND gate receives an input from each moduli's 1-of-N Detector circuit corresponding to each bin in the system's FOV. Pairing is performed in accordance with Figure 3.3. This pairing results in only one of the 64 gates indicating an active state by having a logical 0 as its output. The next step is to provide a more concise output, although a curved 64 segment LED or LCD bar graph could give an intuitive AOA directly from this stage.

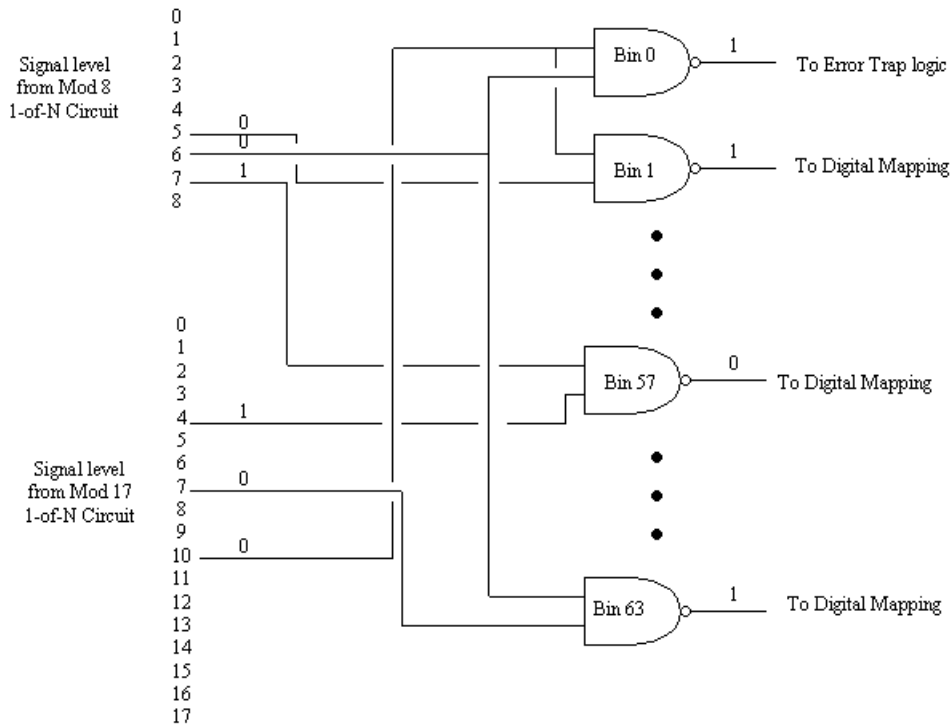


Figure 4.6: Bin Mapping Field.

H. DIGITAL MAPPING

Providing a more concise output than 64 individual logic gates is the function of the Digital Mapping portion of the RSNS Signal Processor. This mapping converts each individual output from the bin mapping field into a binary

representation of its corresponding bin number. As there are 64 unique bins in the FOV of this design, the output is required to be a minimum of six binary bits. This conversion is seen, in part, in Figure 4.7 and accomplished by applying the output of each logic gate from the bin mapping field to the necessary binary digits in the binary output stage. Referring back to the notional implementation of the Bin Mapping field as logical AND gates, this digital mapping would be intuitively implemented in logical OR gates with each providing their output as one of the digits in the binary output. Recalling that the Bin Mapping field is implemented in NAND gates and the lack of the easy commercial availability of any large-input OR gates, six groups of four 8-input NAND gates are utilized with a tree of three 2-input OR gates to map each logic gate from the bin mapping field to the binary output. The DM74LS30 8-Input NAND Gate and the DM74LS32 Quad 2-Input OR Gate chips, both from National Semiconductors, were selected for this application.

Digital mapping could be performed to a variety of values. Mapping could have corresponded to the BCD values of the AOA digits. This would have simplified a digital readout implementation, but would greatly increase the amount of mapping performed by this stage, requiring a 13 bit binary output for mapping three decimal digits plus a sign bit. Mapping to the binary representation of the RSNS bin number was selected due to minimization of binary outputs required and the ease of conversion of the output within simulation programs, thus simplifying generation of the system's transfer function.

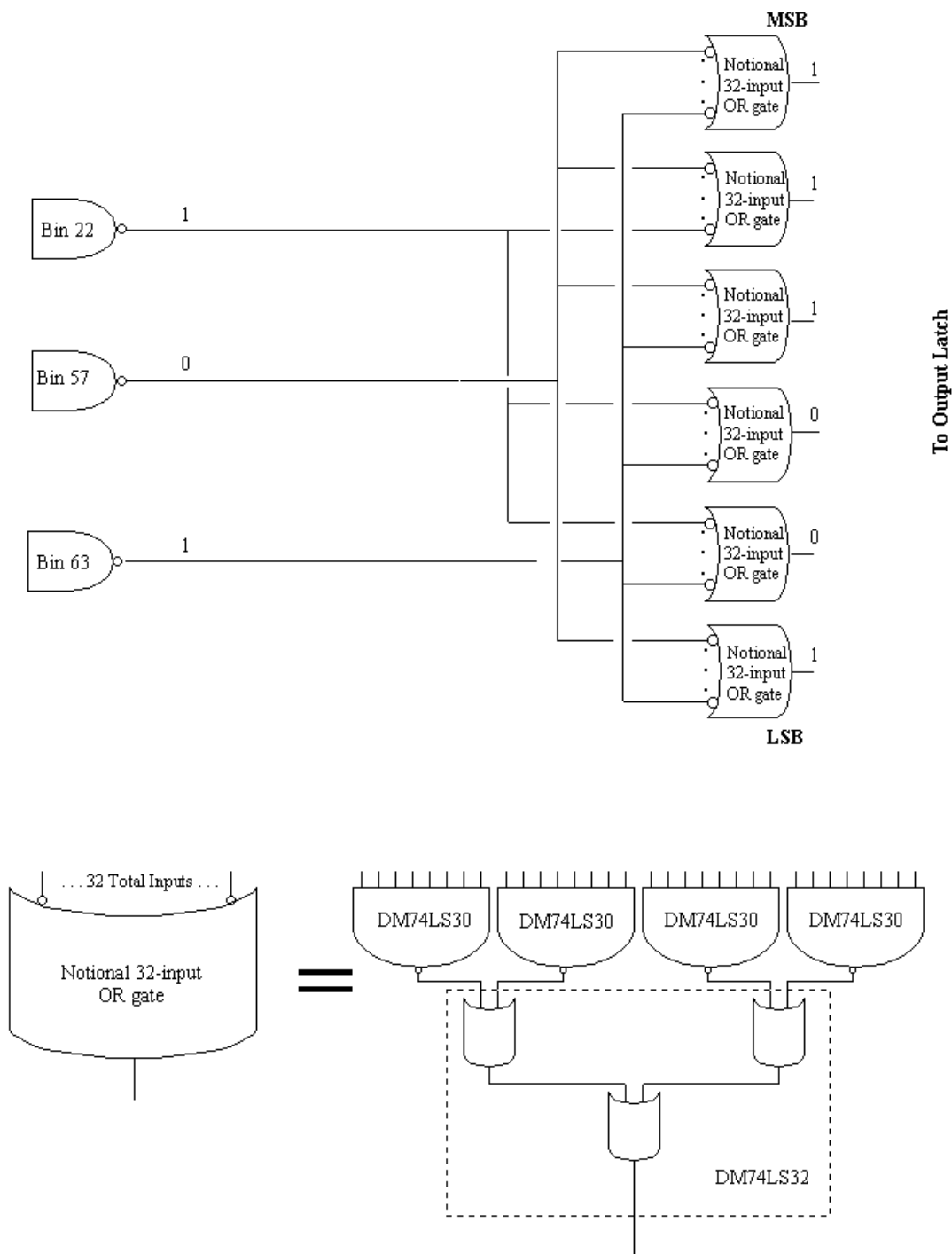


Figure 4.7: Digital Mapping.

An unfortunate result of mapping directly to the RSNS bin number is the potentially large error encountered when

the analog signals do not correspond to an AOA within the system's FOV. As no input is required from the Bin Mapping Field to the Digital Mapping portion to the circuit to generate the representation for bin 0, all erroneous signals are reported as originating from that bin. An error trap has been implemented to alert the operator, and ultimately any system that is automatically processing the signal, to this occurrence. This error trap physically resides on the circuit board with the Decimal Display and implementation will be discussed in Section IV.J.

I. OUTPUT LATCH

Providing a solid output to drive the Decimal Display and the Error Trap while allowing changes to propagate through the digital processor is the function of the Output Latch. The latch is an SN74LS273 identical to the analog signal latch. Commonly known as "pipelining" [8], the necessity for this component was shown when the changing of the Digital Mapping output digits occurred at slightly different times during bin shifts was noted in simulation. This latch is provided with the same 10 kHz clock signal as the analog signal latches.

J. DECIMAL DISPLAY

The Decimal Display provides human readability to the output of the RSNS Signal Processing Circuit. It also provides visual indication of actuation of the Error Trap discussed earlier. As illustrated in Figure 4.8, estimated AOA is displayed to the tenths of degrees by passing the six binary outputs provided by the Output Latch to three PEEL 18CV8 Programmable Logic Devices (PLDs) after an XOR

circuit. This XOR circuit utilizes the most significant bit (MSB) as a toggle bit, taking advantage of the mirror relationship of the AOA about boresight, to enable the PLDs to process five inputs versus six. The software used to program the PEEL 18CV8 PLDs is unable to load the requisite equations utilizing six inputs, thus requiring the XOR circuitry. The PLDs convert the five bit binary output to Binary Coded Decimal (BCD). Details of the PLD programming and implementation are contained in Appendix A. The binary signal is then passed to BCD-to-seven segment decoders to drive three seven segment displays, showing the estimated AOA. The SN7447A BCD-to-Seven-Segment Decoders/Drivers chip from Texas Instruments was selected for this application. The MSB of the output also drives a fourth seven segment display to furnish the negative sign. A fifth seven segment display is utilized to display the error indication.

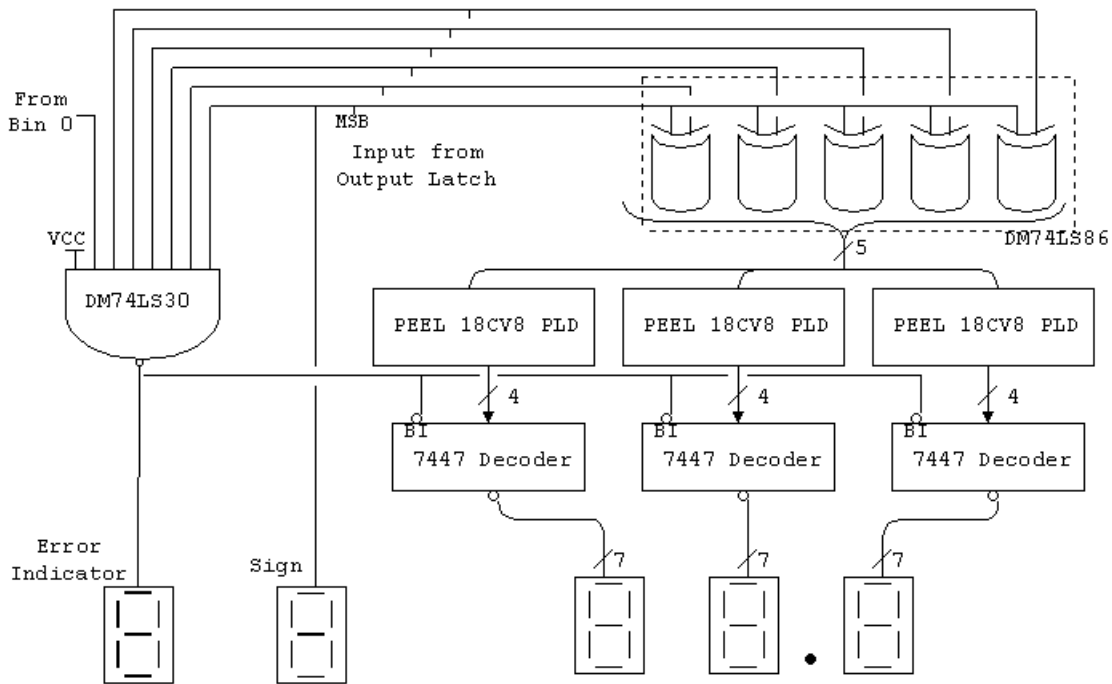


Figure 4.8: Decimal Display block diagram.

Error Trap implementation as shown in Figure 4.8 is accomplished by inverting each output bit from the Output Latch and passing them, along with the output of the NAND from the Bin Mapping Field corresponding to bin 0 through a DM74LS30 8-input NAND gate with one input tied to +5V. This output is used to display an "E" on a seven-segment LED on the Decimal Display. This output also blanks the decimal AOA display by connecting to the 7447's Blanking Input (BI) pin.

K. SYSTEM CONSTRUCTION

Construction of the PCBs starts with dividing the circuit design into the portions to be allocated to each board. This division was necessary primarily due to software limitations within the layout tool that operates in concert with the Multisim circuit design and simulation tool. Ultiboard, the PCB layout tool, has a program limitation of 700 pin connections per board in the software version used. The design contained approximately 1300 pin connections, requiring division into at least two circuit boards. The division of boards selected is roughly along the analog-digital interface. Keeping the analog components as physically close to one another minimized any potential propagation time related errors. The resulting division resulted in the 1-of-N Detector residing on the circuit board with the analog hardware and the remainder of the digital circuitry on a separate circuit board. The digital display and error trap logic reside on a third circuit board.

The analog and digital processing boards were exported individually into Ultiboard from Multisim for PCB layout.

Virtual placement of components was accomplished manually and the routing of traces and vias was performed with the third tool in the software suite, Ultiroute. Care was taken to minimize the lengths of conductors through which the analog signals would be required to travel. The PCBs were contracted to a commercial vendor for manufacture and to a second vendor for installation of the components. The PCBs can be seen in Figures 4.9 and 4.10.

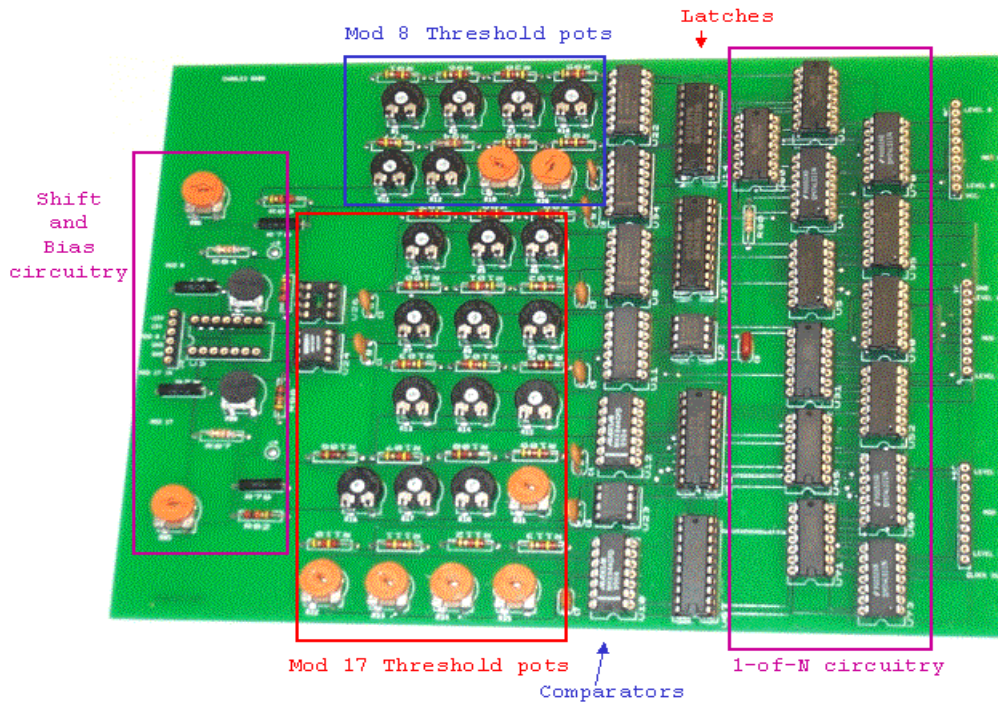


Figure 4.9: RSNS Signal Processing Circuit - Analog PCB.

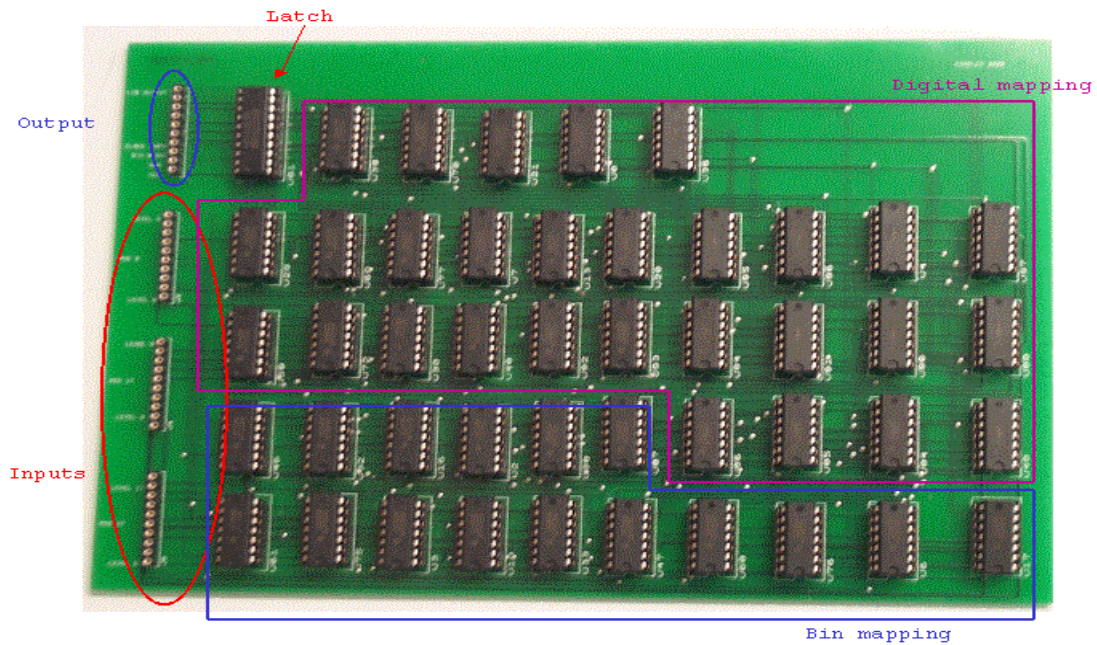


Figure 4.10: RSNS Signal Processing Circuit - Digital PCB.

The Digital Display was constructed locally on a prototype breadboard. The Digital Display is shown in Figure 4.11.

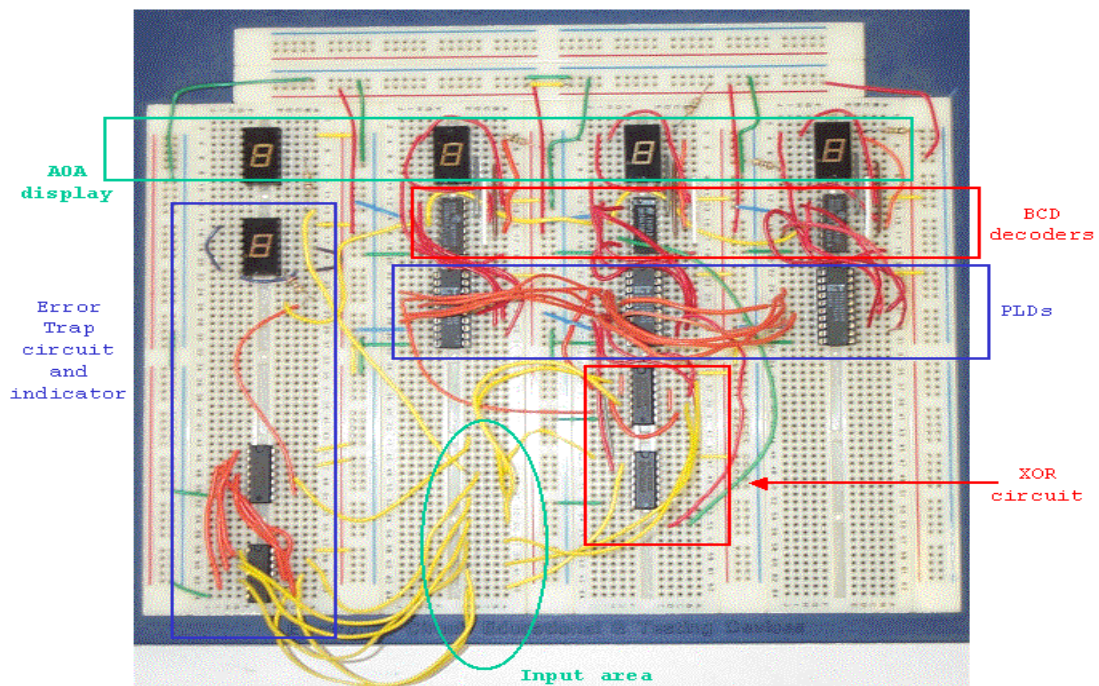


Figure 4.11: Digital Display and circuitry.

V. TESTING AND EVALUATION

A. PRE-FABRICATION SIMULATION

Pre-fabrication testing of the Signal Processing Circuit was performed by simulations using the software selected for the circuit's design, Multisim from Electronics Workbench. Multisim is part of a suite of design tools with an intuitive graphical interface and an extensive database of industry-standard analog, digital and RF components. Multisim exports its simulation results into Excel, making Excel the analysis tool of choice over MatLab.

Initial simulation encompassed verification of the analog circuitry's ability to properly create a thermometer code at the output of the analog signal latches. The next step was a validation of the 1-of-N Detector. This was performed by a visual verification cued by virtual lighted test probes on the Multisim interface screen. The bin mapping field was then designed and tested, again by the visual cues provided by a test probe at the output of each NAND gate. Mapping of each NAND gate representing an RSNS bin to the output stage followed. Verification could now take on the form of reading the binary output and converting that output to bin numbers, allowing a comparison of output to input and development of a system transfer function. The transfer function developed at that time is seen in Figure 5.1.

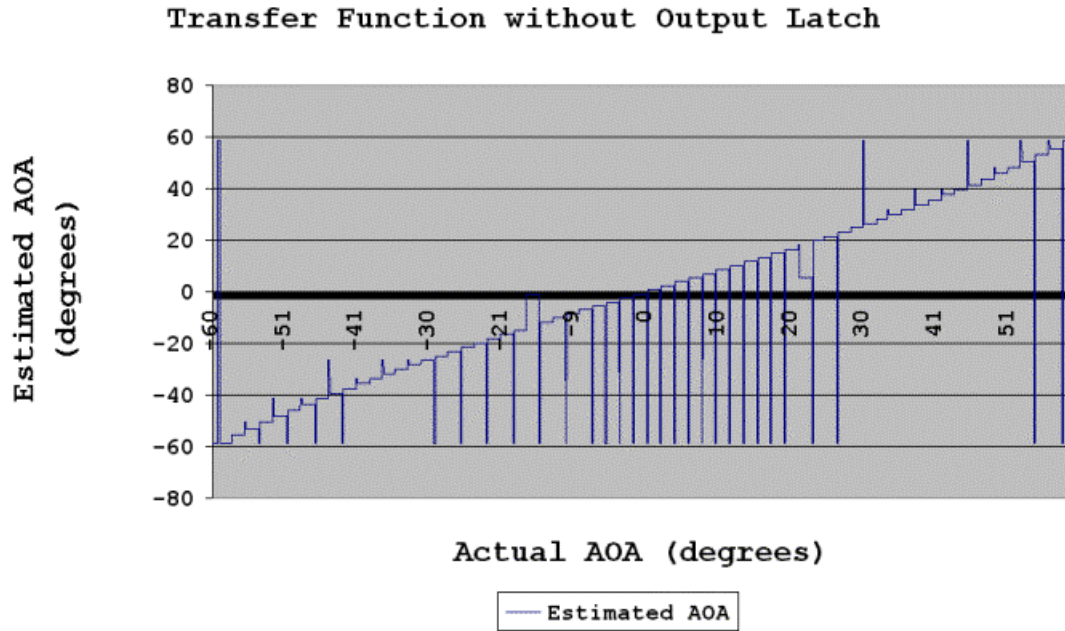


Figure 5.1: Transfer Function of Simulated Circuit before Output Latch Implementation.

Note the irregularities at the initiation point of each successive bin. These spikes represent the transition of more than one bit at minutely different times. These transitions were eliminated by the output latch. The initial implementation utilized six flip-flops of the fourth analog signal latch, but the output latch became a separate entity when it became apparent that the circuit would have to occupy more than one circuit board. The frequency of the latches was initially set at 1kHz. The system transfer function was again determined and is seen in Figure 5.2.

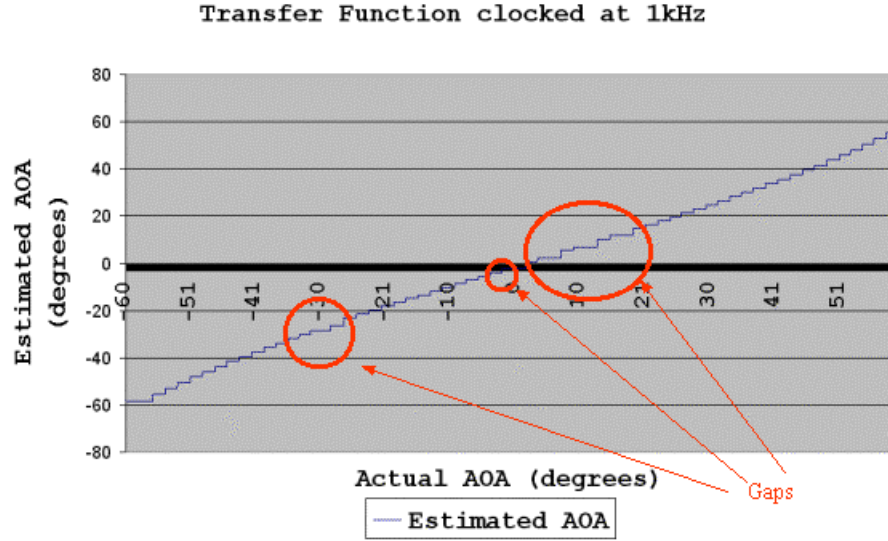


Figure 5.2: Transfer Function of Simulated Circuit with Output Latch clocked at 1kHz.

The transfer function revealed an irregularity in that bins 16, 31, 34, 37 and 40 are skipped. Since the speed of the simulation input was changing at 1 bin/ms, the analog signal was progressing faster than the latch clock frequency. The clock frequency was raised to 10kHz after a determination of clock limitations was performed as listed in Section IV.E. The resulting system transfer function is seen in Figure 5.3. This transfer function illustrates a mapping of actual AOA to estimated AOA with the exception of quantization error discussed in Section III.B. This system resulted in a maximum error of 2.31° and an RMS error of 0.71° .

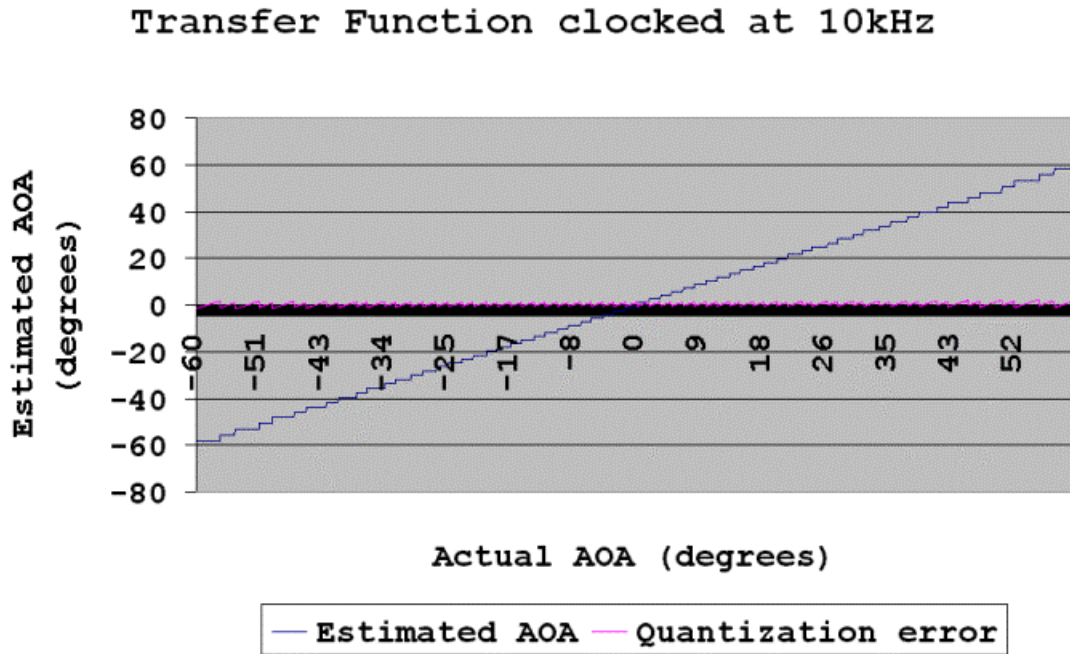


Figure 5.3: Transfer Function of Simulated Circuit after clock adjustment to 10kHz.

All simulations conducted thus far assume theoretical voltage inputs representing the perfect RSNS folding waveforms from the mixers. These waveforms were produced utilizing a MATLAB code that essentially computes the voltage from Equation 2.1 (see Appendix B). Voltages developed by the previously constructed RSNS antenna were measured and are seen in Figures 5.4 and 5.5. Simulation with voltage inputs developed from the RSNS antenna resulted in the system transfer function seen in Figure 5.6. Irregularities in this transfer function are primarily due to relatively minor deficiencies between the perfect and actual folding waveforms. Efforts to remove or minimize these deficiencies are a separate project.

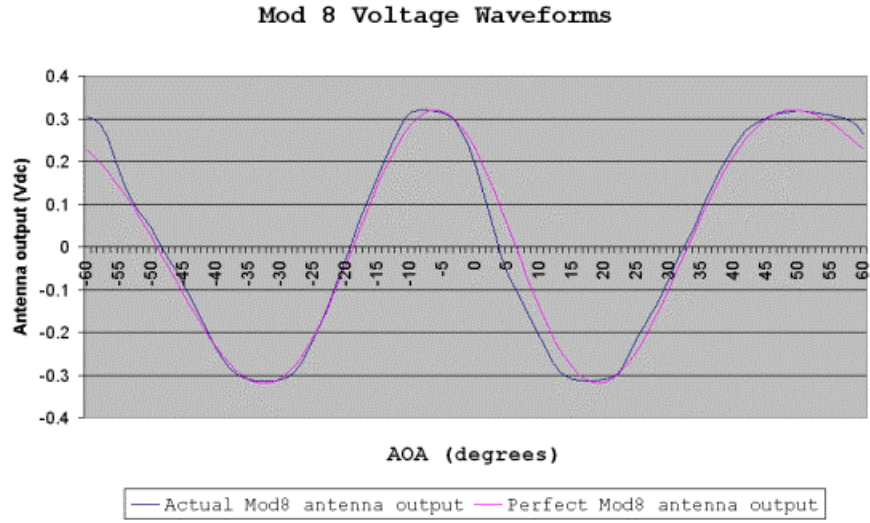


Figure 5.4: Mod 8 Voltage Waveforms for Simulation Input.

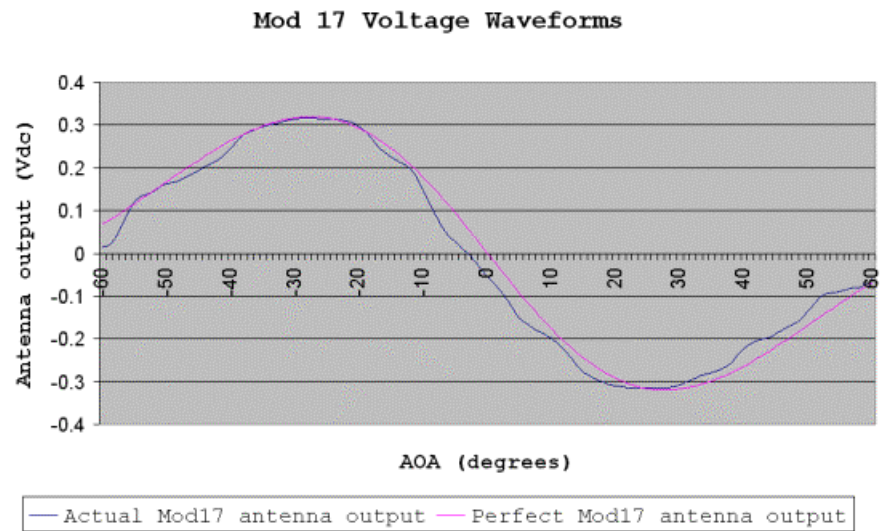


Figure 5.5: Mod 17 Voltage Waveforms for Simulation Input.

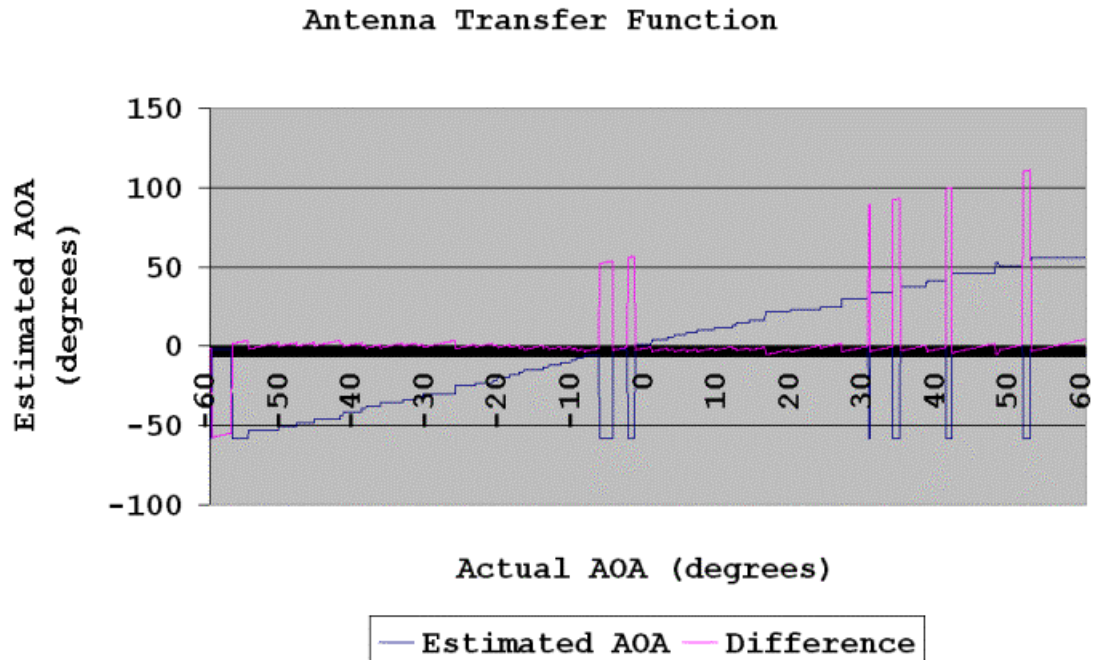


Figure 5.6: Transfer Function of Simulated Circuit with Antenna Data.

B. TESTING SETUP

Testing is performed on each major component of the RSNS DF system as independent units prior to system integration. The fully integrated RSNS DF system was tested in the Naval Postgraduate School Microwave Anechoic Chamber. In the anechoic chamber, a standard gain feed horn transmits a 8 GHz microwave signal generated by a signal generator. The antenna is placed on a pedestal approximately 19 feet from the transmit horn with the microwave components mounted on the back of the antenna's ground plane. A servomotor capable of steps as small as 0.1° rotates the pedestal and indicates its position on the attached personal computer. The signal processing circuit continuously analyzes the received signal and the antenna

mixer output is sampled at each resolution step. The mixer output is carried out of the anechoic chamber to the signal processing circuit and two HP 3478A multimeters. These multimeters sample the antenna output and provide this information both visually and in tabular format in the connected PC. The pedestal position and digital display results are recorded and utilized to determine the system's transfer function.

C. POST-FABRICATION TESTING

After manufacture of the PCBs, testing was performed to verify simulation results. The analog processing circuit board testing included initial alignment of the operational amplifiers and comparator ladder threshold values, plus verification of generation of a correct 1-of-N sequence in response to a ± 320 mVdc applied at each moduli's input. The initial alignment of the analog circuit board revealed the absolute necessity for multi-turn potentiometers in the comparator ladder as the resolution obtainable from the single-turn potentiometers only allowed threshold setting to within about 5 mVdc. Receipt of a correct 1-of-N sequence was verified. The digital processing circuit board testing consisted of manual application of a 1-of-N sequence corresponding to RSNS bins as outlined in Figure 3.3. All input sequences resulted in correct output generation. Testing of the digital display was accomplished by manually applying a six digit binary input and visually verifying a correct AOA indication on the display. The error trap was also exercised to ensure proper operation and anticipated system response of blanking the angular readout and displaying an

"E" on its own seven segment display.

Testing of the complete signal processing circuit was performed in two steps, first driven by perfect RSNS waveforms and then driven by the system's antenna. Waveforms utilized in the testing are seen in Figures 5.7 and 5.8. Integration of the signal processing circuit and application of perfect RSNS waveforms by manually adjusting voltage sources simulating the antenna inputs resulted in a system transfer function seen in Figure 5.9. For illustrative purposes, an activation of the system's error trap and subsequent blanking of the digital display is shown as a lack of estimated AOA on the transfer function and is translated as an AOA of 0° for calculation of the difference between actual AOA and estimated AOA.

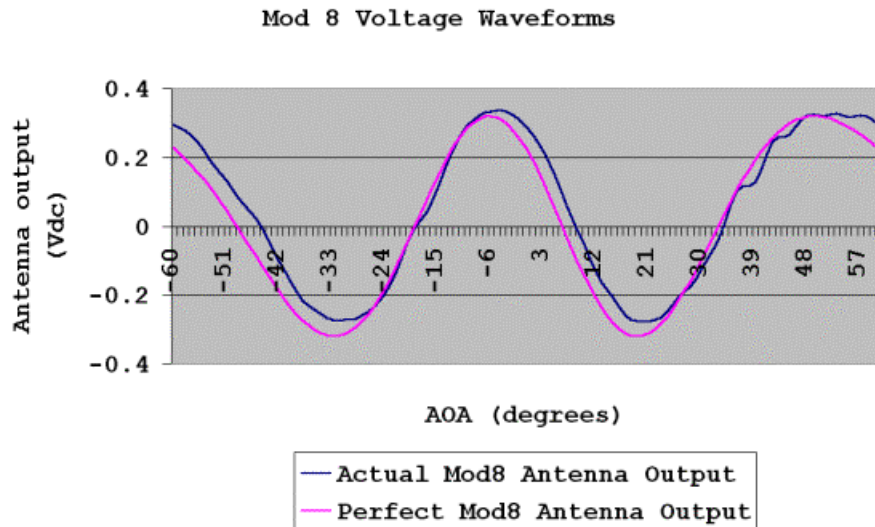


Figure 5.7: Mod8 Waveforms Utilized for System Testing.

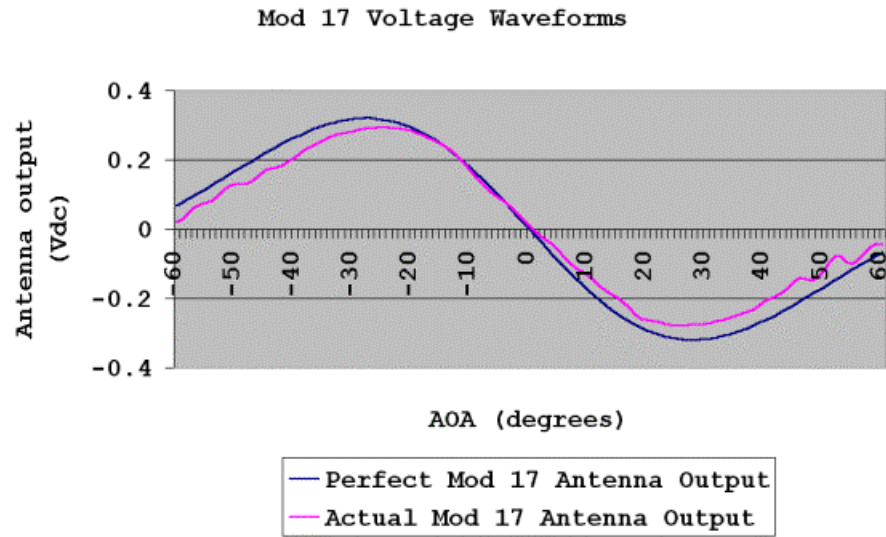


Figure 5.8: Mod17 Waveforms Utilized for System Testing.

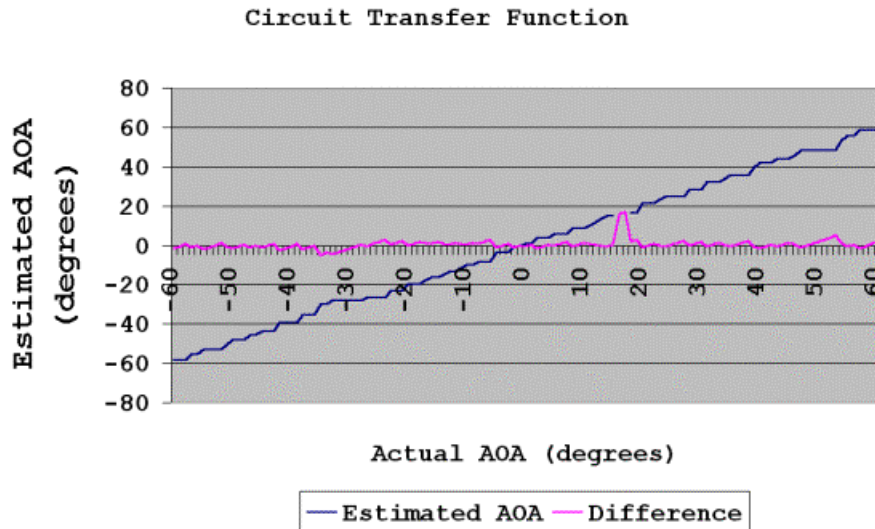


Figure 5.9: Signal Processing Circuit Transfer Function driven with Perfect RSNS Waveforms.

Testing is concluded with the development of the fully integrated RSNS DF system transfer function utilizing the enhanced antenna as the voltage source. Inspection of the

antenna waveforms reveals that the voltage response does not span the full ± 320 mVdc range. As outlined in Section IV.B, the multiplication factor of the Mod 17 analog signal processor was raised to eight and the Mod 8 analog signal processor's multiplication factor was raised to 7.4. The Mod 8 waveform is also not centered around zero, thus requiring adjustment of the DC bias value to 2.3 Vdc versus 2.5 Vdc, also as outlined in Section IV.B. This transfer function, developed as outlined in Section V.B., is seen in Figure 5.10.

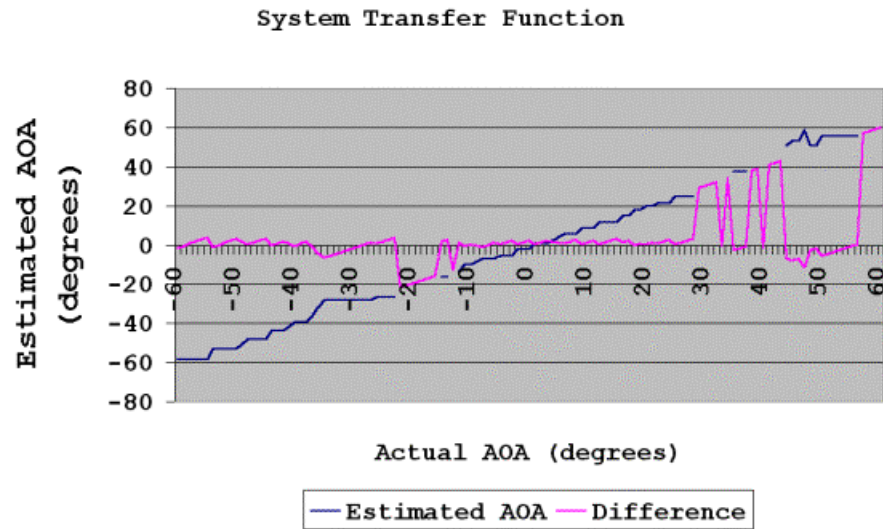


Figure 5.10: Fully Integrated RSNS DF System Transfer Function.

VI. CONCLUSIONS

This research project set out to design, simulate, construct and test the performance of a processing system with a prototype direction finding antenna, utilizing a mixed signal architecture to derive the direction of arrival from an RSNS encoded direction finding antenna. This architecture provides a high resolution, small-baseline array with few phase sampling comparators, based on preprocessing the received signal using the RSNS. This has resulted in a four inch antenna array being able to attain an angular resolution of less than 1.8 degrees with a continuous field of view of 120 degrees. The accompanying electronics occupy two 6 inch by 8 inch printed circuit boards, making this system ideal for platforms with limited space and volume.

The system's transfer function of Figure 5.8 is in good agreement with the ideal case of Figure 3.12. Discrepancies in the system's transfer function are due in large part to the accuracy to which the comparator ladder thresholds can be set in concert with minor imperfections in the antenna's response. This research demonstrates the viability of a direction finding system based on the RSNS.

Future work to be completed on this project should include incorporating the ability to operate in a multi-signal environment plus the capability to have uniform response to a wide range of emitter frequencies.

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APPENDIX A. PLD PROGRAMMING AND IMPLEMENTATION DETAILS

```

MODULE KNRVTR1;
TITLE 'KNRVTR1'

DECLARATIONS

    KNRVTR1                DEVICE    'P18CV8'                ;

"input pins
    G,F,E,D                PIN      1,2,3,4                  ;
    C,B,A,BLANK            PIN      5,6,7,8                  ;

"output pins
    a,b,c,d                PIN      12,13,14,15              ;
    a,b,c,d                IsType   'com'                    ;

"equivalences
    HEX_IN                 =      [G,F,E,D,C,B,A];          "set of inputs
    DISPLAY                 =      [a,b,c,d];                "set of outputs
    H,L,X                   =      1,0,.X.;                  "rename constants
    ANYINPUT                =      [X,X,X,X,X,X,X];
    ANYDISPLAY              =      [X,X,X,X];

"    0    ^b0000 ;    0
"    1    ^b0001 ;    1
"    2    ^b0010 ;    2
"    3    ^b0011 ;    3
"    4    ^b0100 ;    4
"    5    ^b0101 ;    5
"    6    ^b0110 ;    6
"    7    ^b0111 ;    7
"    8    ^b1000 ;    8
"    9    ^b1001 ;    9

TRUTH_TABLE      ( [ BLANK,  HEX_IN ] -> DISPLAY )
                  [  H   ,    0   ] -> ^b0101 ; " 5
                  [  H   ,    1   ] -> ^b0101 ; " 5
                  [  H   ,    2   ] -> ^b0101 ; " 5
                  [  H   ,    3   ] -> ^b0101 ; " 5
                  [  H   ,    4   ] -> ^b0100 ; " 4
                  [  H   ,    5   ] -> ^b0100 ; " 4
                  [  H   ,    6   ] -> ^b0100 ; " 4
                  [  H   ,    7   ] -> ^b0100 ; " 4

```

```

[  H ,      8      ] -> ^b0011 ; " 3
[  H ,      9      ] -> ^b0011 ; " 3
[  H ,     10      ] -> ^b0011 ; " 3
[  H ,     11      ] -> ^b0011 ; " 3
[  H ,     12      ] -> ^b0011 ; " 3
[  H ,     13      ] -> ^b0011 ; " 3
[  H ,     14      ] -> ^b0010 ; " 2
[  H ,     15      ] -> ^b0010 ; " 2

[  H ,     16      ] -> ^b0010 ; " 2
[  H ,     17      ] -> ^b0010 ; " 2
[  H ,     18      ] -> ^b0010 ; " 2
[  H ,     19      ] -> ^b0001 ; " 1
[  H ,     20      ] -> ^b0001 ; " 1
[  H ,     21      ] -> ^b0001 ; " 1
[  H ,     22      ] -> ^b0001 ; " 1
[  H ,     23      ] -> ^b0001 ; " 1
[  H ,     24      ] -> ^b0001 ; " 1
[  H ,     25      ] -> ^b0001 ; " 1
[  H ,     26      ] -> ^b0000 ; " 0
[  H ,     27      ] -> ^b0000 ; " 0
[  H ,     28      ] -> ^b0000 ; " 0
[  H ,     29      ] -> ^b0000 ; " 0
[  H ,     30      ] -> ^b0000 ; " 0
[  H ,     31      ] -> ^b0000 ; " 0

```

```

[  L , ANYINPUT ] -> ^b11111111 ;

```

```

TEST_VECTORS ( [ BLANK,G,F,E,D,C,B,A ] -> [ a,b,c,d ] )
[  1 ,0,0,0,0,0,0,0 ] -> [ 0,1,0,1 ]; " 5
[  1 ,0,0,0,0,0,0,1 ] -> [ 0,1,0,1 ]; " 5
[  1 ,0,0,0,0,0,1,0 ] -> [ 0,1,0,1 ]; " 5
[  1 ,0,0,0,0,0,1,1 ] -> [ 0,1,0,1 ]; " 5
[  1 ,0,0,0,0,1,0,0 ] -> [ 0,1,0,0 ]; " 4
[  1 ,0,0,0,0,1,0,1 ] -> [ 0,1,0,0 ]; " 4
[  1 ,0,0,0,0,1,1,0 ] -> [ 0,1,0,0 ]; " 4
[  1 ,0,0,0,0,1,1,1 ] -> [ 0,1,0,0 ]; " 4
[  1 ,0,0,0,1,0,0,0 ] -> [ 0,0,1,1 ]; " 3
[  1 ,0,0,0,1,0,0,1 ] -> [ 0,0,1,1 ]; " 3
[  1 ,0,0,0,1,0,1,0 ] -> [ 0,0,1,1 ]; " 3
[  1 ,0,0,0,1,0,1,1 ] -> [ 0,0,1,1 ]; " 3
[  1 ,0,0,0,1,1,0,0 ] -> [ 0,0,1,1 ]; " 3
[  1 ,0,0,0,1,1,0,1 ] -> [ 0,0,1,1 ]; " 3
[  1 ,0,0,0,1,1,1,0 ] -> [ 0,0,1,0 ]; " 2

```

```

[ 1 ,0,0,0,1,1,1,1 ] -> [ 0,0,1,0 ]; " 2
[ 1 ,0,0,1,0,0,0,0 ] -> [ 0,0,1,0 ]; " 2
[ 1 ,0,0,1,0,0,0,1 ] -> [ 0,0,1,0 ]; " 2
[ 1 ,0,0,1,0,0,1,0 ] -> [ 0,0,1,0 ]; " 2
[ 1 ,0,0,1,0,0,1,1 ] -> [ 0,0,0,1 ]; " 1
[ 1 ,0,0,1,0,1,0,0 ] -> [ 0,0,0,1 ]; " 1
[ 1 ,0,0,1,0,1,0,1 ] -> [ 0,0,0,1 ]; " 1
[ 1 ,0,0,1,0,1,1,0 ] -> [ 0,0,0,1 ]; " 1
[ 1 ,0,0,1,0,1,1,1 ] -> [ 0,0,0,1 ]; " 1
[ 1 ,0,0,1,1,0,0,0 ] -> [ 0,0,0,1 ]; " 1
[ 1 ,0,0,1,1,0,0,1 ] -> [ 0,0,0,1 ]; " 1
[ 1 ,0,0,1,1,0,1,0 ] -> [ 0,0,0,0 ]; " 0
[ 1 ,0,0,1,1,0,1,1 ] -> [ 0,0,0,0 ]; " 0
[ 1 ,0,0,1,1,1,0,0 ] -> [ 0,0,0,0 ]; " 0
[ 1 ,0,0,1,1,1,0,1 ] -> [ 0,0,0,0 ]; " 0
[ 1 ,0,0,1,1,1,1,0 ] -> [ 0,0,0,0 ]; " 0
[ 1 ,0,0,1,1,1,1,1 ] -> [ 0,0,0,0 ]; " 0

```

END KNVRTR1

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ABEL 5.10 - Device Utilization Chart
08:25:54 19:2

Mon Sep 9

KNVRTR1

Module : 'knvrtr1'

Input files:

| | |
|----------------|---------------|
| ABEL PLA file | : knvrtr1.tt3 |
| Vector file | : knvrtr1.tmv |
| Device library | : P18CV8.dev |

Output files:

| | |
|----------------------|---------------|
| Report file | : knvrtr1.doc |
| Programmer load file | : knvrtr1.jed |

08:25:54 19:2

KNVRTR1

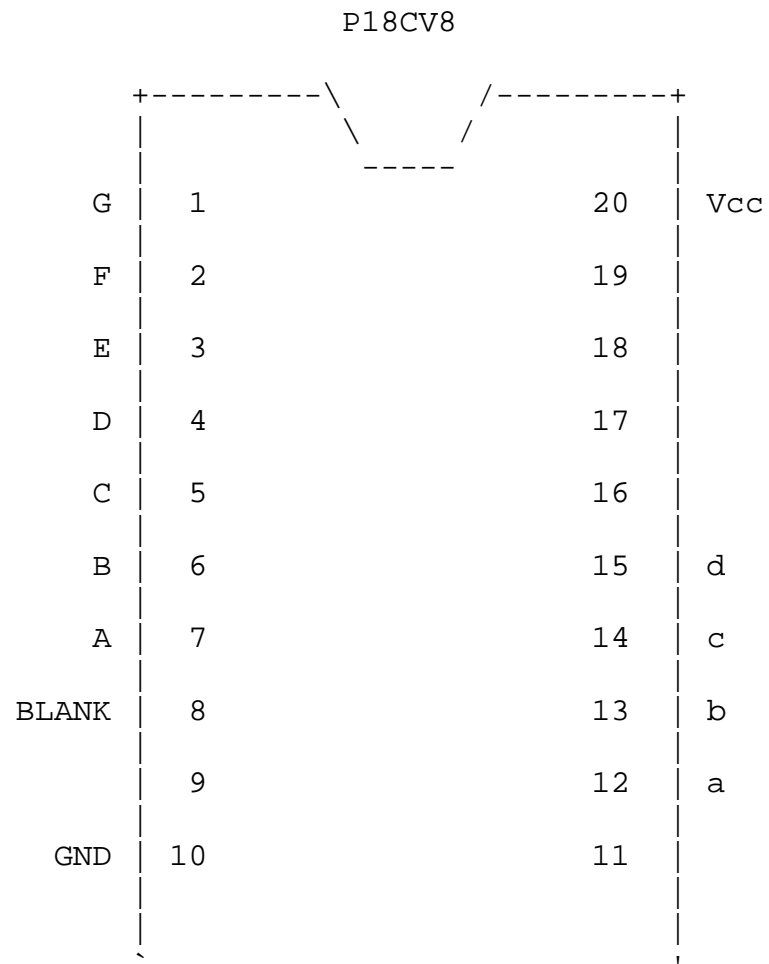
P18CV8 Programmed Logic:

a = (!BLANK);

b = (!D & !E & !F & !G
!BLANK);c = (!A & !C & !D & E & !F & !G
!B & !C & !D & E & !F & !G
D & !E & !F & !G
!BLANK);d = (!B & !C & D & !F & !G
A & B & !C & !D & !F & !G
C & !D & E & !F & !G
!C & !E & !F & !G
!B & D & !E & !F & !G
!BLANK);

KNVRTR1

P18CV8 Chip Diagram:



SIGNATURE: N/A

08:25:55 19:2

KNVRTR1

P18CV8 Resource Allocations:

| Device Resources | Resource Available | Design Requirement | Unused |
|---------------------|-----------------------|-----------------------|-----------|
| ===== | ===== | ===== | ===== |
| Input Pins: | | | |
| Input: | 10 | 8 | 2 (20 %) |
| Output Pins: | | | |
| In/Out: | 8 | 4 | 4 (50 %) |
| Output: | - | - | - |
| Buried Nodes: | | | |
| Input Reg: | - | - | - |
| Pin Reg: | 8 | 0 | 8 (100 %) |
| Buried Reg: | - | - | - |

08:25:55 19:2

KNVRTR1

P18CV8 Product Terms Distribution:

| Signal Name | Pin Assigned | Terms Used | Terms Max | Terms Unused |
|----------------|-----------------|---------------|--------------|-----------------|
| ===== | ===== | ===== | ===== | ===== |
| a | 12 | 1 | 8 | 7 |
| b | 13 | 2 | 8 | 6 |
| c | 14 | 4 | 8 | 4 |
| d | 15 | 6 | 8 | 2 |

==== List of Inputs/Feedbacks ====

| Signal Name | Pin | Pin |
|-------------|-------|--------|
| Type | | |
| ===== | ===== | ===== |
| === | | |
| A | 7 | INPUT |
| B | 6 | INPUT |
| C | 5 | INPUT |
| D | 4 | INPUT |
| E | 3 | INPUT |
| F | 2 | INPUT |
| G | 1 | CLK/IN |
| BLANK | 8 | INPUT |

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ABEL 5.10 - Device Utilization Chart

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KNVRTR1

P18CV8 Unused Resources:

| Pin Number | Pin Type | Product Terms | Flip-flop Type |
|---------------|-------------|------------------|-------------------|
| ===== | ===== | ===== | ===== |
| 9 | INPUT | - | - |
| 11 | INPUT | - | - |
| 16 | BIDIR | NORMAL 8 | D |
| 17 | BIDIR | NORMAL 8 | D |
| 18 | BIDIR | NORMAL 8 | D |
| 19 | BIDIR | NORMAL 8 | D |

```

MODULE KNVRTR2;
TITLE 'KNVRTR2'

```

DECLARATIONS

```

        KNVRTR2                DEVICE    'P18CV8'                ;

"input pins
    G,F,E,D                    PIN       1,2,3,4                ;
    C,B,A,BLANK                PIN       5,6,7,8                ;

    " output pins
        a                      PIN       12                    ;
        a                      IsType    'com,feed_or,pos'      ;

        b                      PIN       13                    ;
        b                      IsType    'com,feed_or,pos'      ;

        c                      PIN       14                    ;
        c                      IsType    'com,feed_or,pos'      ;

        d                      PIN       15                    ;
        d                      IsType    'com,feed_or,pos'      ;

```

EQUATIONS

```

d=!D&!C&(B$A)#!E&!C&(B$A)#D&!C&!(B$A)#E&!D&B&A#C&(B$D)&(B$E
)#!E&C&!B&(A$D)#!E&D&!C      ;

```

```

c=A&(C$D)&(D$E)#!E&!D&B&!A#D&C&B&(E$A)#E&!C&A&!(D$B)#E&C&!B
&A      ;

```

```

b=(B$A)&(E$D)&(C$D)#A&!C&!(E$D)&!(B$D)#C&!B&!(E$D)&(A$D)#(E
&!D&!C&!B&!A#!E&D&C&B&A)      ;

```

```

a=!E&!C&!B&!A # !D&C&!B&!A # D&B&!A&(E$C) # E&!C&B&(D$A)
;

```

```

TEST_VECTORS    ( [ BLANK,G,F,E,D,C,B,A ] -> [ a,b,c,d ] )
[ 1 ,0,0,0,0,0,0,0 ] -> [ 1,0,0,0 ]; " 8
[ 1 ,0,0,0,0,0,0,1 ] -> [ 0,1,0,1 ]; " 5
[ 1 ,0,0,0,0,0,1,0 ] -> [ 0,0,1,1 ]; " 3
[ 1 ,0,0,0,0,0,1,1 ] -> [ 0,0,0,0 ]; " 0

```

```

[ 1 ,0,0,0,0,1,0,0 ] -> [ 1,0,0,0 ]; " 8
[ 1 ,0,0,0,0,1,0,1 ] -> [ 0,1,0,1 ]; " 5
[ 1 ,0,0,0,0,1,1,0 ] -> [ 0,0,1,1 ]; " 3
[ 1 ,0,0,0,0,1,1,1 ] -> [ 0,0,0,1 ]; " 1
[ 1 ,0,0,0,1,0,0,0 ] -> [ 1,0,0,1 ]; " 9
[ 1 ,0,0,0,1,0,0,1 ] -> [ 0,1,1,1 ]; " 7
[ 1 ,0,0,0,1,0,1,0 ] -> [ 0,1,0,1 ]; " 5
[ 1 ,0,0,0,1,0,1,1 ] -> [ 0,0,1,1 ]; " 3
[ 1 ,0,0,0,1,1,0,0 ] -> [ 0,0,0,1 ]; " 1
[ 1 ,0,0,0,1,1,0,1 ] -> [ 0,0,0,0 ]; " 0
[ 1 ,0,0,0,1,1,1,0 ] -> [ 1,0,0,0 ]; " 8
[ 1 ,0,0,0,1,1,1,1 ] -> [ 0,1,1,0 ]; " 6
[ 1 ,0,0,1,0,0,0,0 ] -> [ 0,1,0,0 ]; " 4
[ 1 ,0,0,1,0,0,0,1 ] -> [ 0,0,1,1 ]; " 3
[ 1 ,0,0,1,0,0,1,0 ] -> [ 0,0,0,1 ]; " 1
[ 1 ,0,0,1,0,0,1,1 ] -> [ 1,0,0,1 ]; " 9
[ 1 ,0,0,1,0,1,0,0 ] -> [ 1,0,0,0 ]; " 8
[ 1 ,0,0,1,0,1,0,1 ] -> [ 0,1,1,0 ]; " 6
[ 1 ,0,0,1,0,1,1,0 ] -> [ 0,1,0,0 ]; " 4
[ 1 ,0,0,1,0,1,1,1 ] -> [ 0,0,1,1 ]; " 3
[ 1 ,0,0,1,1,0,0,0 ] -> [ 0,0,0,1 ]; " 1
[ 1 ,0,0,1,1,0,0,1 ] -> [ 0,0,0,0 ]; " 0
[ 1 ,0,0,1,1,0,1,0 ] -> [ 1,0,0,0 ]; " 8
[ 1 ,0,0,1,1,0,1,1 ] -> [ 0,1,1,1 ]; " 7
[ 1 ,0,0,1,1,1,0,0 ] -> [ 0,1,0,1 ]; " 5
[ 1 ,0,0,1,1,1,0,1 ] -> [ 0,0,1,1 ]; " 3
[ 1 ,0,0,1,1,1,1,0 ] -> [ 0,0,1,0 ]; " 2
[ 1 ,0,0,1,1,1,1,1 ] -> [ 0,0,0,0 ]; " 0

```

END KNVRTR2

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ABEL 5.10 - Device Utilization Chart

Thu Sep 19

09:24:20 19:2

KNVRTR2

Module : 'knvrtr2'

Input files:

| | |
|----------------|---------------|
| ABEL PLA file | : knvrtr2.tt3 |
| Vector file | : knvrtr2.tmv |
| Device library | : P18CV8.dev |

Output files:

| | |
|----------------------|---------------|
| Report file | : knvrtr2.doc |
| Programmer load file | : knvrtr2.jed |

09:24:20 19:2

KNVRTR2

P18CV8 Programmed Logic:


```

a      = (  !D & C & !B & !A
            #   !D & !C & B & A & E
            #   D & !C & B & !A & E
            #   D & C & B & !A & !E
            #   !C & !B & !A & !E );

```

```

b      = (  !D & C & !B & A
            #   D & !C & B & A & E
            #   !D & C & B & !A & E
            #   D & C & !B & !A & E
            #   !D & !C & !B & !A & E
            #   D & C & B & A & !E
            #   !C & !B & A & !E
            #   D & !C & B & !A & !E );

```

```

c      = (  D & !C & B & A
            #   !D & C & A & E
            #   !D & !B & A & E
            #   C & !B & A & E
            #   D & C & B & !A & E
            #   D & !C & A & !E
            #   D & B & A & !E
            #   !D & B & !A & !E );

```

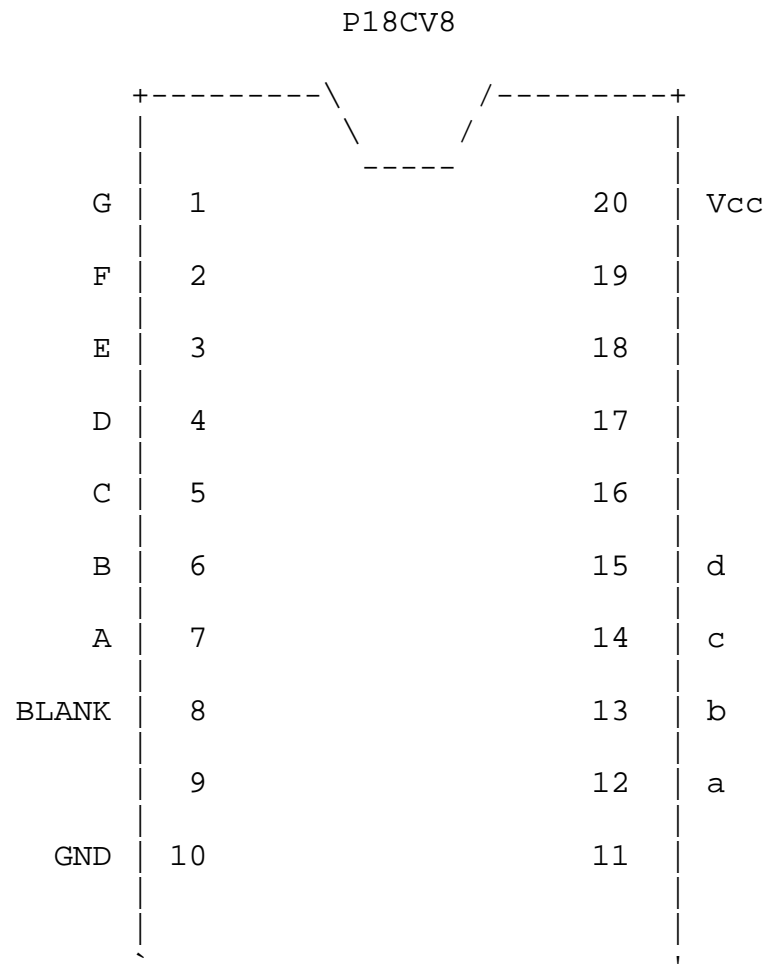
```

d      = !(  D & C & B
            #   !D & !B & !A
            #   !D & C & !B & E
            #   D & !C & !B & A & E
            #   !D & C & !A & E
            #   D & B & !A & E
            #   D & C & A & !E
            #   !D & !C & B & A & !E );

```

KNVRTR2

P18CV8 Chip Diagram:



SIGNATURE: N/A

09:24:21 19:2

KNVRTR2

P18CV8 Resource Allocations:

| Device Resources | Resource Available | Design Requirement | Unused |
|---------------------|-----------------------|-----------------------|-----------|
| ===== | ===== | ===== | ===== |
| ==== | | | |
| Input Pins: | | | |
| Input: | 10 | 5 | 5 (50 %) |
| Output Pins: | | | |
| In/Out: | 8 | 4 | 4 (50 %) |
| Output: | - | - | - |
| Buried Nodes: | | | |
| Input Reg: | - | - | - |
| Pin Reg: | 8 | 0 | 8 (100 %) |
| Buried Reg: | - | - | - |

KNVRTR2

P18CV8 Product Terms Distribution:

| Signal Name | Pin Assigned | Terms Used | Terms Max | Terms Unused |
|----------------|-----------------|---------------|--------------|-----------------|
| ===== | ===== | ===== | ===== | ===== |
| a | 12 | 5 | 8 | 3 |
| b | 13 | 8 | 8 | 0 |
| c | 14 | 8 | 8 | 0 |
| d | 15 | 8 | 8 | 0 |

==== List of Inputs/Feedbacks ====

| Signal Name | Pin | Pin |
|-------------|-------|-------|
| Type | | |
| ===== | ===== | ===== |
| === | | |
| D | 4 | INPUT |
| C | 5 | INPUT |
| B | 6 | INPUT |
| A | 7 | INPUT |
| E | 3 | INPUT |

KNVRTR2

P18CV8 Unused Resources:

| Pin Number | Pin Type | Product Terms | Flip-flop Type |
|---------------|-------------|------------------|-------------------|
| ===== | ===== | ===== | ===== |
| 2 | INPUT | - | - |
| 8 | INPUT | - | - |
| 9 | INPUT | - | - |
| 11 | INPUT | - | - |
| 16 | BIDIR | NORMAL 8 | D |
| 17 | BIDIR | NORMAL 8 | D |
| 18 | BIDIR | NORMAL 8 | D |
| 19 | BIDIR | NORMAL 8 | D |

```

MODULE KNVRTR3;
TITLE 'KNVRTR3'

```

DECLARATIONS

```

        KNVRTR3                DEVICE    'P18CV8'                ;

"input pins
    G,F,E,D                    PIN       1,2,3,4                ;
    C,B,A,BLANK                PIN       5,6,7,8                ;

"output pins
    a,b,c,d                    PIN       12,13,14,15            ;
    a,b,c,d                    IsType    'com'                  ;

"equivalences
    HEX_IN                     =        [G,F,E,D,C,B,A];        "set of inputs
    DISPLAY                     =        [a,b,c,d];              "set of outputs
    H,L,X                       =        1,0,.X.;               "rename constants
    ANYINPUT                    =        [X,X,X,X,X,X,X,X];
    ANYDISPLAY                  =        [X,X,X,X,X];

"    0    ^b0000 ; 0
"    1    ^b0001 ; 1
"    2    ^b0010 ; 2
"    3    ^b0011 ; 3
"    4    ^b0100 ; 4
"    5    ^b0101 ; 5
"    6    ^b0110 ; 6
"    7    ^b0111 ; 7
"    8    ^b1000 ; 8
"    9    ^b1001 ; 9

```

```

TRUTH_TABLE      ( [ BLANK,  HEX_IN  ] ->  DISPLAY )
    [  H  ,      0  ] -> ^b0101 ; " 5
    [  H  ,      1  ] -> ^b0111 ; " 7
    [  H  ,      2  ] -> ^b0000 ; " 0
    [  H  ,      3  ] -> ^b0101 ; " 5
    [  H  ,      4  ] -> ^b0001 ; " 1
    [  H  ,      5  ] -> ^b1000 ; " 8
    [  H  ,      6  ] -> ^b0111 ; " 7
    [  H  ,      7  ] -> ^b0110 ; " 6
    [  H  ,      8  ] -> ^b0101 ; " 5
    [  H  ,      9  ] -> ^b0101 ; " 5
    [  H  ,     10  ] -> ^b0110 ; " 6
    [  H  ,     11  ] -> ^b0111 ; " 7

```

```

[   H   ,    12   ] -> ^b1001 ; " 9
[   H   ,    13   ] -> ^b0001 ; " 1
[   H   ,    14   ] -> ^b0011 ; " 3
[   H   ,    15   ] -> ^b0101 ; " 5

[   H   ,    16   ] -> ^b1000 ; " 8
[   H   ,    17   ] -> ^b0001 ; " 1
[   H   ,    18   ] -> ^b0100 ; " 4
[   H   ,    19   ] -> ^b1000 ; " 8
[   H   ,    20   ] -> ^b0001 ; " 1
[   H   ,    21   ] -> ^b0101 ; " 5
[   H   ,    22   ] -> ^b1001 ; " 9
[   H   ,    23   ] -> ^b0011 ; " 3
[   H   ,    24   ] -> ^b0111 ; " 7
[   H   ,    25   ] -> ^b0001 ; " 1
[   H   ,    26   ] -> ^b0110 ; " 6
[   H   ,    27   ] -> ^b0000 ; " 0
[   H   ,    28   ] -> ^b0100 ; " 4
[   H   ,    29   ] -> ^b1001 ; " 9
[   H   ,    30   ] -> ^b0011 ; " 3
[   H   ,    31   ] -> ^b1000 ; " 8

```

```

[   L   , ANYINPUT ] -> ^b11111111 ;

```

```

TEST_VECTORS ( [ BLANK,G,F,E,D,C,B,A ] -> [ a,b,c,d ] )
[   1   ,0,0,0,0,0,0,0 ] -> [ 0,1,0,1 ]; " 5
[   1   ,0,0,0,0,0,0,1 ] -> [ 0,1,1,1 ]; " 7
[   1   ,0,0,0,0,0,1,0 ] -> [ 0,0,0,0 ]; " 0
[   1   ,0,0,0,0,0,1,1 ] -> [ 0,1,0,1 ]; " 5
[   1   ,0,0,0,0,1,0,0 ] -> [ 0,0,0,1 ]; " 1
[   1   ,0,0,0,0,1,0,1 ] -> [ 1,0,0,0 ]; " 8
[   1   ,0,0,0,0,1,1,0 ] -> [ 0,1,1,1 ]; " 7
[   1   ,0,0,0,0,1,1,1 ] -> [ 0,1,1,0 ]; " 6
[   1   ,0,0,0,1,0,0,0 ] -> [ 0,1,0,1 ]; " 5
[   1   ,0,0,0,1,0,0,1 ] -> [ 0,1,0,1 ]; " 5
[   1   ,0,0,0,1,0,1,0 ] -> [ 0,1,1,0 ]; " 6
[   1   ,0,0,0,1,0,1,1 ] -> [ 0,1,1,1 ]; " 7
[   1   ,0,0,0,1,1,0,0 ] -> [ 1,0,0,1 ]; " 9
[   1   ,0,0,0,1,1,0,1 ] -> [ 0,0,0,1 ]; " 1
[   1   ,0,0,0,1,1,1,0 ] -> [ 0,0,1,1 ]; " 3
[   1   ,0,0,0,1,1,1,1 ] -> [ 0,1,0,1 ]; " 5
[   1   ,0,0,1,0,0,0,0 ] -> [ 1,0,0,0 ]; " 8
[   1   ,0,0,1,0,0,0,1 ] -> [ 0,0,0,1 ]; " 1
[   1   ,0,0,1,0,0,1,0 ] -> [ 0,1,0,0 ]; " 4

```

```

[ 1 ,0,0,1,0,0,1,1 ] -> [ 1,0,0,0 ]; " 8
[ 1 ,0,0,1,0,1,0,0 ] -> [ 0,0,0,1 ]; " 1
[ 1 ,0,0,1,0,1,0,1 ] -> [ 0,1,0,1 ]; " 5
[ 1 ,0,0,1,0,1,1,0 ] -> [ 1,0,0,1 ]; " 9
[ 1 ,0,0,1,0,1,1,1 ] -> [ 0,0,1,1 ]; " 3
[ 1 ,0,0,1,1,0,0,0 ] -> [ 0,1,1,1 ]; " 7
[ 1 ,0,0,1,1,0,0,1 ] -> [ 0,0,0,1 ]; " 1
[ 1 ,0,0,1,1,0,1,0 ] -> [ 0,1,1,0 ]; " 6
[ 1 ,0,0,1,1,0,1,1 ] -> [ 0,0,0,0 ]; " 0
[ 1 ,0,0,1,1,1,0,0 ] -> [ 0,1,0,0 ]; " 4
[ 1 ,0,0,1,1,1,0,1 ] -> [ 1,0,0,1 ]; " 9
[ 1 ,0,0,1,1,1,1,0 ] -> [ 0,0,1,1 ]; " 3
[ 1 ,0,0,1,1,1,1,1 ] -> [ 1,0,0,0 ]; " 8

```

END KNVRTR3

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ABEL 5.10 - Device Utilization Chart

Mon Sep 9

08:26:38 19:2

KNVRTR3

Module : 'knvrtr3'

Input files:

ABEL PLA file : knvrtr3.tt3
Vector file : knvrtr3.tmv
Device library : P18CV8.dev

Output files:

Report file : knvrtr3.doc
Programmer load file : knvrtr3.jed

08:26:38 19:2

KNVRTR3

P18CV8 Programmed Logic:

```

-----
a      = (  A & C & D & E & !F & !G
           #   !A & B & C & !D & E & !F & !G
           #   A & B & !C & !D & E & !F & !G
           #   !A & !B & !C & !D & E & !F & !G
           #   !A & !B & C & D & !E & !F & !G
           #   A & !B & C & !D & !E & !F & !G
           #   !BLANK );

```

```

b      = (  !A & !C & D & !F & !G
           #   !A & B & !C & E & !F & !G
           #   !A & !B & D & E & !F & !G
           #   A & !B & C & !D & E & !F & !G
           #   A & B & !E & !F & !G
           #   !B & !C & !E & !F & !G
           #   B & C & !D & !E & !F & !G
           #   !BLANK );

```

```

c      = (  !A & B & D & !F & !G
           #   A & B & C & !D & !F & !G
           #   !A & !C & D & E & !F & !G
           #   B & !C & D & !E & !F & !G
           #   B & C & !D & !E & !F & !G
           #   A & !B & !C & !D & !E & !F & !G
           #   !BLANK );

```

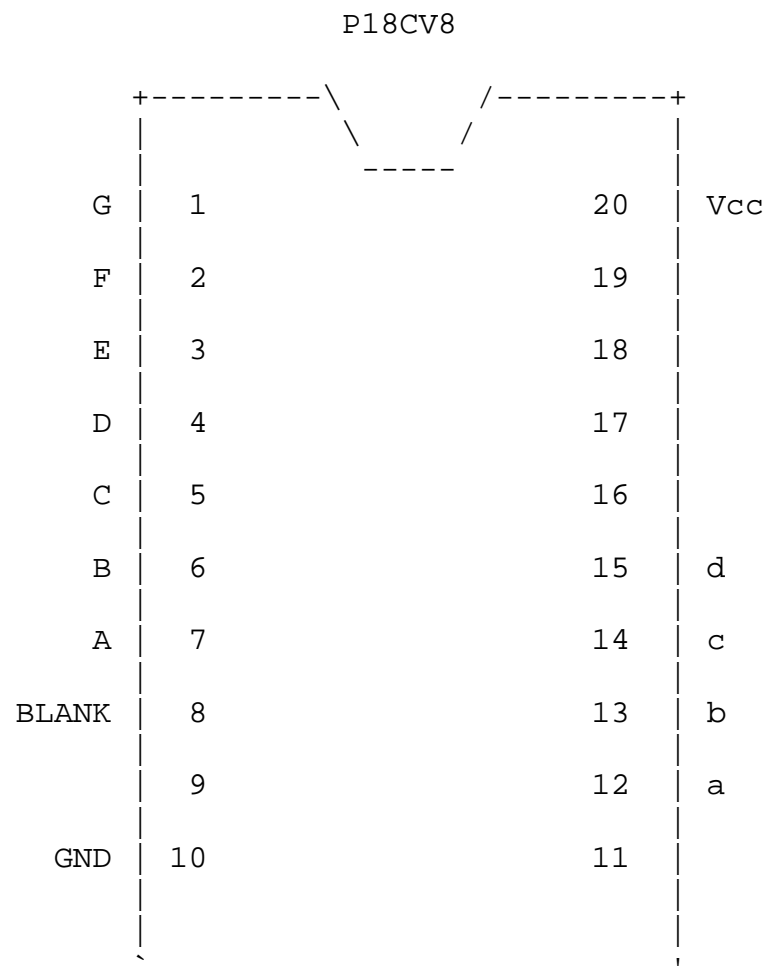
```

d      = (  !A & B & C & !F & !G
           #   !B & !C & D & !F & !G
           #   A & !B & E & !F & !G
           #   C & !D & E & !F & !G
           #   !A & !B & !E & !F & !G
           #   A & !C & !E & !F & !G
           #   A & D & !E & !F & !G
           #   !BLANK );

```

KNVRTR3

P18CV8 Chip Diagram:



SIGNATURE: N/A

08:26:39 19:2

KNVRTR3

P18CV8 Resource Allocations:

| Device Resources | Resource Available | Design Requirement | Unused |
|---------------------|-----------------------|-----------------------|-----------|
| ===== | ===== | ===== | ===== |
| ==== | | | |
| Input Pins: | | | |
| Input: | 10 | 8 | 2 (20 %) |
| Output Pins: | | | |
| In/Out: | 8 | 4 | 4 (50 %) |
| Output: | - | - | - |
| Buried Nodes: | | | |
| Input Reg: | - | - | - |
| Pin Reg: | 8 | 0 | 8 (100 %) |
| Buried Reg: | - | - | - |

08:26:39 19:2

KNVRTR3

P18CV8 Product Terms Distribution:

| Signal Name | Pin Assigned | Terms Used | Terms Max | Terms Unused |
|----------------|-----------------|---------------|--------------|-----------------|
| ===== | ===== | ===== | ===== | ===== |
| a | 12 | 7 | 8 | 1 |
| b | 13 | 8 | 8 | 0 |
| c | 14 | 7 | 8 | 1 |
| d | 15 | 8 | 8 | 0 |

==== List of Inputs/Feedbacks ====

| Signal Name | Pin | Pin |
|-------------|-------|--------|
| Type | | |
| ===== | ===== | ===== |
| ==== | | |
| A | 7 | INPUT |
| B | 6 | INPUT |
| C | 5 | INPUT |
| D | 4 | INPUT |
| E | 3 | INPUT |
| F | 2 | INPUT |
| G | 1 | CLK/IN |
| BLANK | 8 | INPUT |

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ABEL 5.10 - Device Utilization Chart

Mon Sep 9

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KNVRTR3

P18CV8 Unused Resources:

| Pin Number | Pin Type | Product Terms | Flip-flop Type |
|---------------|-------------|------------------|-------------------|
| ===== | ===== | ===== | ===== |
| 9 | INPUT | - | - |
| 11 | INPUT | - | - |
| 16 | BIDIR | NORMAL 8 | D |
| 17 | BIDIR | NORMAL 8 | D |
| 18 | BIDIR | NORMAL 8 | D |
| 19 | BIDIR | NORMAL 8 | D |

APPENDIX B. MATLAB CODE CREATING PERFECT WAVEFORMS

[From Ref 4]

%RSNS8 WITH SHIFTING

% LT Nathan York, 15 December 2000

% Generates the simulated folding waveform. Two element arrays assumed.

% Can accept normalized mixer output for comparison to simulated waveform.

% Plots folding waveforms for simulated and measured data.

% m = modulus; d = spacing (m); f = frequency

clear

N=2;

f=8.0e9; c=3e8; wavl=c/f;

k=2*pi/wavl;

rad=pi/180;

sf=sqrt(3)/2 % sf is the scale factor

% ffd is forced phase difference to align signal to required zero crossing

ffd=45; %original is 45!

% number of moduli in array design and their values

mm=[8 17]; nm=length(mm);

disp('moduli are: '),disp(mm)

% specify a modulus to plot

m=8;

% M is Dynamic Range

M=64;

% nf is number of folds

nf=M/(2*m*N);

% determines required element spacing

d=nf*wavl/sf/2;

% start, stop, increment angles

start=-90; stop=90; inc=0.1;

N=floor((stop-start)/inc)+1;

for n=1:N;

thd(n)=start+(n-1)*inc; thr=thd(n)*rad;

arg(n)=k*d*sin(thr);

% mixer output

mx(n)=cos(arg(n)+(ffd)*(pi/180));

end

load rsns14.dat

both8=[thd' mx'];

```

save simu8.dat both8 -ascii

figure(1)
hold
plot(thd,mx,'b');
plot(rsns14(:,1),rsns14(:,3),'r')

hold off
xlabel('Angle of Arrival'),ylabel('Normalized Mixer Output');
grid
xlabel('Angle of Arrival (degrees)')
ylabel('Normalized Mixer Output')
title(['Modulus 8, with ffd = ',num2str(ffd)])
legend('Simulated','Measured',0)
axis([-90,90,-1,1])
orient landscape

temp=rsns14(:,3);
temp1=rot90(temp);
left=temp1-mx;
zero=0;

figure (2)
hold
plot(thd,mx,'b');
plot(rsns14(:,1),rsns14(:,3),'r')
plot(thd,left,'g');
plot(thd,zero,'k');
xlabel('Angle of Arrival (degrees)')
ylabel('Normalized Mixer Output')
legend('Simulated','Measured','Difference',0)
axis([-90,90,-1,1])
grid
title('Modulus 8, Measured values - Expected values')

```


[From Ref 4]

%RSNS17 WITH SCALING

% LT Nathan York, 15 December 2000

% Generates the simulated folding waveform. Two element arrays assumed.

% Can accept normalized mixer output for comparison to simulated waveform.

% Plots folding waveforms for simulated and measured data.

% m = modulus; d = spacing (m); f = frequency

clear

N=2;

f=8e9; c=3e8; wavl=c/f;

sf=.8746; %sqrt(3)/2

k=2*pi/wavl;

rad=pi/180;

% ffd is forced phase difference to align signal to required zero crossing

ffd=90 %original is 90!

m=17;

% M is Dynamic Range

M=64;

% nf is number of folds

nf=M/(2*m*N);

% calculation of required element spacing

d=nf*wavl/sf/2;

% start, stop, increment angles

start=-90; stop=90; inc=0.1;

N=floor((stop-start)/inc)+1;

for n=1:N;

thd(n)=start+(n-1)*inc; thr=thd(n)*rad;

arg(n)=k*d*sin(thr);

% mixer output

mx(n)=cos(arg(n)+(ffd)*(pi/180));

end

load rsns11.dat;

load rsns14.dat;

load PAT9.dat;

load PAT10.dat;

load pat10a.dat

both17=[thd' mx'];

save simul7.dat both17 -ascii;

figure(3)

```

hold
plot(thd,mx,'b');

% LABVIEW Output has mod 17 mixer output in second column.
% Normalization technique puts normalized mixer output in third
column.
plot(rsns14(:,4),rsns14(:,6),'r')

hold off
xlabel('Angle of Arrival (degrees)'),ylabel('Normalized Mixer Output');
grid
title(['Modulus 17, with ffd = ',num2str(ffd)])
legend('Simulated','Measured',0)
xlabel('Angle of Arrival (degrees)')
ylabel('Normalized Mixer Output')
axis([-90,90,-1,1])
orient landscape

temp=rsns14(:,6);
temp1=rot90(temp);
left=temp1-mx;
zero=0;

figure (4)
hold
plot(thd,mx,'b');
plot(rsns14(:,4),rsns14(:,6),'r')
plot(thd,left,'g')
plot(thd,zero,'k')
legend('Simulated','Measured','Difference',0)
grid
xlabel('Angle of Arrival (degrees)')
ylabel('Normalized Mixer Output')
axis([-90,90,-1,1])
title('Modulus 17, Measured values - Expected values')

```

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